KONGU ENGINEERING COLLEGE

(Autonomous Institution Affiliated to Anna University, Chennai)

PERUNDURAI ERODE – 638 060

TAMILNADU INDIA

Estd : 1984

REGULATIONS, CURRICULUM & SYLLABI - 2020

(CHOICE BASED CREDIT SYSTEM)

(For the students admitted during 2020 - 2021 and onwards)

MASTER OF ENGINEERING DEGREE
IN
VLSI DESIGN

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

KONGU
Assuring the Best

INDEX

KONGU ENGINEERING COLLEGE
PERUNDURAI ERODE – 638 060
(Autonomous)

INSTITUTE VISION

To be a centre of excellence for development and dissemination of knowledge in Applied Sciences, Technology, Engineering and Management for the Nation and beyond.

INSTITUTE MISSION

We are committed to value based Education, Research and Consultancy in Engineering and Management and to bring out technically competent, ethically strong and quality professionals to keep our Nation ahead in the competitive knowledge intensive world.

QUALITY POLICY

We are committed to

- Provide value based quality education for the development of students as competent and responsible citizens.
- Contribute to the nation and beyond through research and development
- Continuously improve our services

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To be a centre of excellence for development and dissemination of knowledge in Electronics and Communication Engineering for the Nation and beyond

MISSION

Department of Electronics and Communication Engineering is committed to:

MS1:	To impart industry and research based quality education for developing value based electronics and communication engineers
MS2:	To enrich the academic activities by continual improvement in the teaching learning process
MS3:	To infuse confidence in the minds of students to develop as entrepreneurs
MS4:	To develop expertise for consultancy activities by providing thrust for Industry Institute Interaction
MS5:	To endeavour for constant upgradation of technical expertise for producing competent professionals to cater to the needs of the society and to meet the global challenges

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

Post Graduates of Electronics and Communication Engineering will

PEO1:	Succeed in industry and research by applying knowledge of modeling, design and fabrication techniques of Integrated Circuits
PEO2:	Identify, design and analyze solutions to solve real world problems in VLSI design
PEO3:	Demonstrate soft skills , professional and ethical values and aptitude for life long learning needed for a successful professional career

MAPPING OF MISSION STATEMENTS (MS) WITH PEOs

MS\PEO	PEO1	PEO2	PEO3
MS1	3	3	3
MS2	2	3	2
MS3	3	3	3
MS4	2	3	1
MS5	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

PROGRAM OUTCOMES (POs)	
M.E(VLSI Design) Graduates will be able to:	
PO1:	Independently carry out research/investigation and development work to solve practical problems
PO2:	Write and present a substantial technical report /document
PO3:	Demonstrate a degree of mastery over the areas of VLSI Systems, IC fabrication, design, testing, verification and prototype development focusing on applications
PO4:	Integrate multiple sub-systems to develop System On Chip and optimize its performance
PO5:	Identify and apply appropriate Electronic Design Automation (EDA) tool to create innovative products/ systems to solve real world problems in VLSI domain
PO6:	Apply appropriate managerial and technical skills in the domain of VLSI design incorporating safety and sustainability to become a successful Professional / entrepreneur through lifelong learning

MAPPING OF PEOs WITH POs

PEO\PO	PO1	PO2	PO3	PO4	PO5	PO6
PEO1	3	3	3	3	3	2
PEO2	3	1	3	3	3	2
PEO3	3	1	3	3	3	3

1 – Slight, 2 – Moderate, 3 – Substantial

KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638060

(An Autonomous Institution Affiliated to Anna University)

REGULATIONS 2020

CHOICE BASED CREDIT SYSTEM AND OUTCOME BASED EDUCATION

MASTER OF ENGINEERING (ME) / MASTER OF TECHNOLOGY (MTech) DEGREE PROGRAMMES

These regulations are applicable to all candidates admitted into ME/MTech Degree programmes from the academic year 2020 – 2021 onwards.

1. DEFINITIONS AND NOMENCLATURE

In these Regulations, unless otherwise specified:

i. "University" means ANNA UNIVERSITY, Chennai.

ii. "College" means KONGU ENGINEERING COLLEGE.

iii. "Programme" means Master of Engineering (ME) / Master of Technology (MTech) Degree programme

iv. "Branch" means specialization or discipline of ME/MTech Degree programme, like Construction Engineering and Management, Information Technology, etc.

v. "Course" means a Theory / Theory cum Practical / Practical course that is normally studied in a semester like Engineering Design Methodology, Machine Learning Techniques, etc.

vi. "Credit" means a numerical value allocated to each course to describe the candidate's workload required per week.

vii. "Grade" means the letter grade assigned to each course based on the marks range specified.

viii. "Grade point" means a numerical value (0 to 10) allocated based on the grade assigned to each course.

ix. "Principal" means Chairman, Academic Council of the College.

x. "Controller of Examinations" means authorized person who is responsible for all examination related activities of the College.

xi. "Head of the Department" means Head of the Department concerned of the College.

2. PROGRAMMES AND BRANCHES OF STUDY

The following programmes and branches of study approved by Anna University, Chennai and All India Council for Technical Education, New Delhi are offered by the College.

Programme	Branch
ME	Construction Engineering and Management
	Structural Engineering
	Engineering Design
	Mechatronics Engineering
	VLSI Design
	Embedded Systems
	Power Electronics and Drives
	Control and Instrumentation Engineering
	Computer Science and Engineering
MTech	Information Technology
	Chemical Engineering
	Food Technology

3. ADMISSION REQUIREMENTS

Candidates seeking admission to the first semester of the ME/MTech Degree programme shall be required to have passed an appropriate qualifying Degree Examination of Anna University or any examination of any other University or authority accepted by the Anna University, Chennai as equivalent thereto, subject to amendments as may be made by the Anna University, Chennai from time to time. The candidates shall also be required to satisfy all other conditions of admission prescribed by the Anna University, Chennai and Directorate of Technical Education, Chennai from time to time.

4. STRUCTURE OF PROGRAMMES

4.1 Categorisation of Courses

The ME / MTech programme shall have a curriculum with syllabi comprising of theory, theory cum practical, practical courses in each semester and project work, internship,etc that have been approved by the respective Board of Studies and Academic Council of the College. All the programmes have well defined Programme Outcomes (PO) and Programme Educational Objectives (PEOs) as per Outcome Based Education (OBE). The content of each course is designed based on the Course Outcomes (CO). The courses shall be categorized as follows:

i. Foundation Courses (FC)

ii. Professional Core (PC) Courses

iii. Professional Elective (PE) Courses

iv. Open Elective (OE) Courses

v. Employability Enhancement Courses (EC) like Innovative Project, Internship cum Project work in Industry or elsewhere, Project Work

4.2 Credit Assignment

Each course is assigned certain number of credits as follows:

Contact period per week	Credits
1 Lecture / Tutorial Period	1
2 Practical Periods	1
2 Project Work Periods	1
40 Training /Internship Periods	1

The minimum number of credits to complete the ME/MTech programme is 72.

4.3 Employability Enhancement Courses

A candidate shall be offered with the employability enhancement courses like innovative project, internship cum project work and project work during the programme to gain/exhibit the knowledge/skills.

4.3.1 Innovative Project

A candidate shall earn two credits by successfully completing the project by using his/her innovations in second semester during his/her programme.

4.3.2 Internship cum Project Work

The curriculum enables a candidate to go for full time internship during the third semester and can earn credits through it for his/her academics vide clause 7.6 and clause 7.12. Such candidate shall earn the minimum number of credits as mentioned in the third semester of the curriculum other than internship by either fast track mode or through approved courses in online mode or by self study mode. Such candidate can earn the number of credits for the internship same as that of Project Work in the third semester. Assessment procedure is to be followed as specified in the guidelines approved by the Academic Council.

4.3.4 Project Work

A candidate shall earn nine credits by successfully completing the project work in fourth semester during the programme inside the campus or in industries.

4.4 Value Added Courses / Online Courses / Self Study Courses

The candidates may optionally undergo Value Added Courses / Online Courses / Self Study Courses as elective courses.

4.4.1 **Value Added Courses:** Value Added courses each with One / Two credits shall be offered by the college with the prior approval from respective Board of Studies. A candidate can earn a maximum of three credits through value added courses during the entire duration of the programme.

4.4.2 **Online Courses:** Candidates may be permitted to earn credits for online courses, offered by NPTEL / SWAYAM / a University / Other Agencies, approved by respective Board of Studies.

4.4.3 **Self Study Courses:** The Department may offer an elective course as a self study course. The syllabus of the course shall be approved by the respective Board of Studies. However, mode of assessment for a self study course will be the same as that used for other courses. The candidates shall study such courses on their own under the guidance of member of the faculty. Self study course is limited to one per semester.

4.4.4 The elective courses in the final year may be exempted if a candidate earns the required credits vide clause 4.4.1, 4.4.2 and 4.4.3 by registering the required number of courses in advance (up to second semester).

4.4.5 A candidate can earn a maximum of 15 credits through all value added courses, online courses and self study courses.

4.5 Flexibility to Add or Drop Courses

4.5.1 A candidate has to earn the total number of credits specified in the curriculum of the respective programme of study in order to be eligible to obtain the degree. However, if the candidate wishes, then the candidate is permitted to earn more than the total number of credits prescribed in the curriculum of the candidate's programme.

4.5.2 From the second to fourth semesters the candidates have the option of registering for additional elective/Honors courses or dropping of already registered additional elective/Honors courses within two weeks from the start of the semester. Add / Drop is only an option given to the candidates. Total number of credits of such courses during the entire programme of study cannot exceed six.

4.6 Maximum number of credits the candidate can enroll in a particular semester cannot exceed 30 credits.

4.7 The blend of different courses shall be so designed that the candidate at the end of the programme would have been trained not only in his / her relevant professional field but also would have developed to become a socially conscious human being.

4.8 The medium of instruction, examinations and project report shall be English.

5. DURATION OF THE PROGRAMME

5.1 A candidate is normally expected to complete the ME / MTech Degree programme in 4 consecutive semesters (2 Years), but in any case not more than 8 semesters (4 Years).

5.2 Each semester shall consist of a minimum of 90 working days including continuous assessment test period. The Head of the Department shall ensure that every teacher imparts instruction as per the number of periods specified in the syllabus for the course being taught.

5.3 The total duration for completion of the programme reckoned from the commencement of the first semester to which the candidate was admitted shall not exceed the maximum duration specified in clause 5.1 irrespective of the period of break of study (vide clause 11) or prevention (vide clause 9) in order that the candidate may be eligible for the award of the degree (vide clause 16). Extension beyond the prescribed period shall not be permitted.

6. COURSE REGISTRATION FOR THE EXAMINATION

6.1 Registration for the end semester examination is mandatory for courses in the current semester as well as for the arrear courses failing which the candidate will not be permitted to move on to the higher semester. This will not be applicable for the courses which do not have an end semester examination.

6.2 The candidates who need to reappear for the courses which have only continuous assessment shall enroll for the same in the subsequent semester, when offered next, and repeat the course. In this case, the candidate shall attend the classes, satisfy the attendance requirements (vide clause 8), earn continuous assessment marks. This will be considered as an attempt for the purpose of classification.

6.3 If a candidate is prevented from writing end semester examination of a course due to lack of attendance, the candidate has to attend the classes, when offered next, and fulfill the attendance requirements as per clause 8 and earn continuous assessment marks. If the course, in which the candidate has a lack of attendance, is an elective, the candidate may register for the same or any other elective course in the subsequent semesters and that will be considered as an attempt for the purpose of classification.

7. ASSESSMENT AND EXAMINATION PROCEDURE FOR AWARDING MARKS

7.1 The ME/MTech programmes consist of Theory Courses, Theory cum Practical courses, Practical courses, Innovative Project, Internship cum Project work and Project Work. Performance in each course of study shall be evaluated based on (i) Continuous Assessments (CA) throughout the semester and (ii) End Semester Examination (ESE) at the end of the semester except for the courses which are evaluated based on continuous assessment only. Each course shall be evaluated for a maximum of 100 marks as shown below:

Sl. No.	Category of Course	Continuous Assessment Marks	End Semester Examination
1.	Theory / Practical	50	50
2.	Theory cum Practical	The distribution of marks shall be decided based on the credit weightage assigned to theory and practical components respectively.	

3.	Innovative Project/ Project Work / Internship cum Project Work	50	50
4.	Value Added Course	The distribution of marks shall be decided based on the credit the credit weightage assigned	---
5.	All other Courses		

7.2 Examiners for setting end semester examination question papers for theory courses, theory cum practical courses and practical courses and evaluating end semester examination answer scripts, project works, innovative project and internships shall be appointed by the Controller of Examinations after obtaining approval from the Principal.

7.3 Theory Courses

For all theory courses out of 100 marks, the continuous assessment shall be 50 marks and the end semester examination shall be for 50 marks. However, the end semester examinations shall be conducted for 100 marks and the marks obtained shall be reduced to 50. The continuous assessment tests shall be conducted as per the schedule laid down in the academic schedule. Three tests shall be conducted for 50 marks each and reduced to 30 marks each. The total of the continuous assessment marks and the end semester examination marks shall be rounded off to the nearest integer.

7.3.1 The assessment pattern for awarding continuous assessment marks shall be as follows:

Sl. No.	Type	Max. Marks	Remarks
1.	Test – I	30	Average o f best two
	Test – II	30	
	Test - III	30	
2.	Tutorial	15	Should be of Open Book/Objective Type. Average of best 4 (or more, depending on the nature of the course, as may be approved by Principal)
3.	Assignment / Paper Presentation in Conference / Seminar / Comprehension / Activity based learning / Class notes	05	To be assessed by the Course Teacher based on any one type.
	Total	50	Rounded off to the one decimal place

However, the assessment pattern for awarding the continuous assessment marks may be changed based on the nature of the course and is to be approved by the Principal.

7.3.2 A reassessment test or tutorial covering the respective test or tutorial portions may be conducted for those candidates who were absent with valid reasons (Sports or any other reason approved by the Principal).

7.3.3 The end semester examination for theory courses shall be for duration of three hours.

7.4 Theory cum Practical Courses

For courses involving theory and practical components, the evaluation pattern as per the clause 7.1 shall be followed. Depending on the nature of the course, the end semester examination shall be conducted for theory and the practical components. The apportionment of continuous assessment and end semester examination marks shall be decided based on the credit weightage assigned to theory and practical components approved by Principal.

7.5 Practical Courses

For all practical courses out of 100 marks, the continuous assessment shall be for 50 marks and the end semester examination shall be for 50 marks. Every exercise / experiment shall be evaluated based on the candidate's performance during the practical class and the candidate's records shall be maintained.

7.5.1 The assessment pattern for awarding continuous assessment marks for each course shall be decided by the course coordinator based on rubrics of that particular course, and shall be based on rubrics for each experiment.

7.6 Project Work

7.6.1 Project work shall becarried out individually. Candidates can opt for full time internship (vide clause 7.8) in lieu of project work in third semester. The project work is mandatory for all the candidates.

7.6.2 The Head of the Department shall constitute review committee for project work. There shall be three assessments by the review committee during the semester. The candidate shall make presentation on the progress made by him/her before the committee.

7.6.3 The continuous assessment and end semester examination marks for Project Work and the Viva-Voce Examination shall be distributed as below.

Continuous Assessment (Max. 50 Marks)						End Semester Examination (Max. 50 Marks)			
Review I (Max..10 Marks)		Review II (Max.. 20 Marks)		Review III (Max. 20 Marks)		Report Evaluation (Max. 20 Marks)	Viva - Voce (Max. 30 Marks)		
Rv. Com	Guide	Review Committee (excluding guide)	Guide	Review Committee (excluding guide)	Guide	Ext. Exr.	Guide	Exr. 1	Exr. 2
5	5	10	10	10	10	20	10	10	10

7.6.4 The Project Report prepared according to approved guidelines and duly signed by the Guide and Project Co-ordinator shall be submitted to Head of the

Department. A candidate must submit the project report within the specified date as per the academic schedule of the semester. If the project report is not submitted within the specified date then the candidate is deemed to have failed in the Project Work and redo it in the subsequent semester. This applies to both Internship cum Project work and Project work.

7.6.5 If a candidate fails to secure 50% of the continuous assessment marks in the project work, he / she shall not be permitted to submit the report for that particular semester and shall have to redo it in the subsequent semester and satisfy attendance requirements.

7.6.6 Every candidate shall, based on his/her project work, publish a paper in a reputed journal or reputed conference in which full papers are published after usual review. A copy of the full paper accepted and proof for that shall be produced at the time of evaluation.

7.6.7 The project work shall be evaluated based on the project report submitted by the candidate in the respective semester and viva-voce examination by a committee consisting of two examiners and guide of the project work.

7.6.8 If a candidate fails to secure 50 % of the end semester examination marks in the project work, he / she shall be required to resubmit the project report within 30 days from the date of declaration of the results and a fresh viva-voce examination shall be conducted as per clause 7.6.7.

7.6.9 A copy of the approved project report after the successful completion of viva-voce examination shall be kept in the department library.

7.7 Innovative Project

The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding clause 7.6.6.

7.8 Internship cum Project Work

Each candidate shall submit a brief report about the internship undergone and a certificate issued from the organization concerned at the time of Viva-voce examination to the review committee. The evaluation method shall be same as that of the Project Work as per clause 7.6 excluding 7.6.6.

7.9 Value Added Course

Two assessments shall be conducted during the value added course duration by the offering department concerned.

7.10 Online Course

The Board of Studies will provide methodology for the evaluation of the online courses. The Board can decide whether to evaluate the online courses through continuous assessment and end semester examination or through end semester examination only. In case of credits earned through online mode from NPTEL / SWAYAM / a University / Other Agencies approved by Chairman, Academic Council, the credits may be transferred and grades shall be assigned accordingly.

7.11 Self Study Course

The member of faculty approved by the Head of the Department shall be responsible for periodic monitoring and evaluation of the course. The course shall be evaluated through continuous assessment and end semester examination. The evaluation methodology shall be the same as that of a theory course.

7.12 Audit Course

A candidate may be permitted to register for specific course not listed in his/her programme curriculum and without undergoing the rigors of getting a 'good' grade, as an Audit course, subject to the following conditions.

The candidate can register only one Audit course in a semester starting from second semester subject to a maximum of two courses during the entire programme of study. Such courses shall be indicated as 'Audit' during the time of Registration itself. Only courses currently offered for credit to the candidates of other branches can be audited.

A course appearing in the curriculum of a candidate cannot be considered as an audit course. However, if a candidate has already met the Professional Elective and Open Elective credit requirements as stipulated in the curriculum, then, a Professional Elective or an Open Elective course listed in the curriculum and not taken by the candidate for credit can be considered as an audit course.

Candidates registering for an audit course shall meet all the assessment and examination requirements (vide clause 7.3) applicable for a credit candidate of that course. Only if the candidate obtains a performance grade, the course will be listed in the semester Grade Sheet and in the Consolidated Grade Sheet along with the grade SF (Satisfactory). Performance grade will not be shown for the audit course.

Since an audit course has no grade points assigned, it will not be counted for the purpose of GPA and CGPA calculations.

8. REQUIREMENTS FOR COMPLETION OF A SEMESTER

8.1 A candidate who has fulfilled the following conditions shall be deemed to have satisfied the requirements for completion of a semester and permitted to appear for the examinations of that semester.

8.1.1 Ideally, every candidate is expected to attend all classes and secure 100 % attendance. However, a candidate shall secure not less than 80 % (after rounding off to the nearest integer) of the overall attendance taking into account the total number of working days in a semester.

8.1.2 A candidate who could not satisfy the attendance requirements as per clause 8.1.1 due to medical reasons (hospitalization / accident / specific illness) but has secured not less than 70 % in the current semester may be permitted to appear for the current semester examinations with the approval of the Principal on payment of a condonation fee as may be fixed by the authorities from time to time. The medical certificate needs to be submitted along with the leave application. A candidate can avail this provision only twice during the entire duration of the degree programme.

8.1.3 In addition to clause 8.1.1 or 8.1.2, a candidate shall secure not less than 60 % attendance in each course.

8.1.4 A candidate shall be deemed to have completed the requirements of study of any semester only if he/she has satisfied the attendance requirements (vide clause 8.1.1 to 8.1.3) and has registered for examination by paying the prescribed fee.

8.1.5 Candidate's progress is satisfactory.

8.1.6 Candidate's conduct is satisfactory and he/she was not involved in any indisciplined activities in the current semester.

8.2. The candidates who do not complete the semester as per clauses from 8.1.1 to 8.1.6 except 8.1.3 shall not be permitted to appear for the examinations at the end of the semester and not be permitted to go to the next semester. They have to repeat the incomplete semester in next academic year.

8.3 The candidates who satisfy the clause 8.1.1 or 8.1.2 but do not complete the course as per clause 8.1.3 shall not be permitted to appear for the end semester examination of that course alone. They have to repeat the incomplete course in the subsequent semester when it is offered next.

9. REQUIREMENTS FOR APPEARING FOR END SEMESTER EXAMINATION

9.1 A candidate shall normally be permitted to appear for end semester examination of the current semester if he/she has satisfied the semester completion requirements as per clause 8, and has registered for examination in all courses of that semester. Registration is mandatory for current semester examinations as well as for arrear examinations failing which the candidate shall not be permitted to move on to the higher semester.

9.2 When a candidate is deputed for a National / International Sports event during End Semester examination period, supplementary examination shall be conducted for such a candidate on return after participating in the event within a reasonable period of time. Such appearance shall be considered as first appearance.

9.3 A candidate who has already appeared for a course in a semester and passed the examination is not entitled to reappear in the same course for improvement of letter grades / marks.

10. PROVISION FOR WITHDRAWAL FROM EXAMINATIONS

10.1 A candidate may, for valid reasons, be granted permission to withdraw from appearing for the examination in any regular course or all regular courses registered in a particular semester. Application for withdrawal is permitted only once during the entire duration of the degree programme.

10.2 The withdrawal application shall be valid only if the candidate is otherwise eligible to write the examination (vide clause 9) and has applied to the Principal for permission prior to the last examination of that semester after duly recommended by the Head of the Department.

10.3 The withdrawal shall not be considered as an appearance for deciding the eligibility of a candidate for First Class with Distinction/First Class.

10.4 If a candidate withdraws a course or courses from writing end semester examinations, he/she shall register the same in the subsequent semester and write the end semester examinations. A final semester candidate who has withdrawn shall be permitted to appear for supplementary examination to be conducted within reasonable time as per clause 14.

10.5 The final semester candidate who has withdrawn from appearing for project viva-voce for genuine reasons shall be permitted to appear for supplementary viva-voce examination within reasonable time with proper application to Controller of Examinations and on payment of prescribed fee.

11. PROVISION FOR BREAK OF STUDY

11.1 A candidate is normally permitted to avail the authorised break of study under valid reasons (such as accident or hospitalization due to prolonged ill health or any other valid reasons) and to rejoin the programme in a later semester. He/She shall apply in advance to the Principal, through the Head of the Department, stating the reasons therefore, in any case, not later than the last date for registering for that semester examination. A candidate is permitted to avail the authorised break of study only once during the entire period of study for a maximum period of one year. However, in extraordinary situation the candidate may apply for additional break of study not exceeding another one year by paying prescribed fee for the break of study.

11.2 The candidates permitted to rejoin the programme after break of study / prevention due to lack of attendance shall be governed by the rules and regulations in force at the time of rejoining.

11.3 The candidates rejoining in new Regulations shall apply to the Principal in the prescribed format through Head of the Department at the beginning of the readmitted semester itself for prescribing additional/equivalent courses, if any, from any semester of the regulations in-force, so as to bridge the curriculum in-force and the old curriculum.

11.4 The total period of completion of the programme reckoned from the commencement of the semester to which the candidate was admitted shall not exceed the maximum period specified in clause 5 irrespective of the period of break of study in order to qualify for the award of the degree.

11.5 If any candidate is prevented for want of required attendance, the period of prevention shall not be considered as authorized break of study.

11.6 If a candidate has not reported to the college for a period of two consecutive semesters without any intimation, the name of the candidate shall be deleted permanently from the college enrollment. Such candidates are not entitled to seek readmission under any circumstances.

12. PASSING REQUIREMENTS

12.1 A candidate who secures not less than 50 % of total marks (continuous assessment and end semester examination put together) prescribed for the course with a minimum of 50 % of the marks prescribed for the end semester examination in all category of courses vide clause 7.1 except for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course in the examination.

12.2 A candidate who secures not less than 50 % in continuous assessment marks prescribed for the courses which are evaluated based on continuous assessment only shall be declared to have successfully passed the course. If a candidate secures less than 50% in the continuous assessment marks, he / she shall have to re-enroll for the same in the subsequent semester and satisfy the attendance requirements.

12.3 For a candidate who does not satisfy the clause 12.1, the continuous assessment marks secured by the candidate in the first attempt shall be retained and considered valid for subsequent attempts. However, from the fourth attempt onwards the marks scored in the end semester examinations alone shall be considered, in which case the candidate shall secure minimum 50 % marks in the end semester examinations to satisfy the passing requirements, but the grade awarded shall be only the lowest passing grade irrespective of the marks secured.

13. REVALUATION OF ANSWER SCRIPTS

A candidate shall apply for a photocopy of his / her semester examination answer script within a reasonable time from the declaration of results, on payment of a prescribed fee by submitting the proper application to the Controller of Examinations. The answer script shall be pursued and justified jointly by a faculty member who has handled the course and the course coordinator and recommended for revaluation. Based on the recommendation, the candidate can register for revaluation through proper application to the Controller of Examinations. The Controller of Examinations will arrange for revaluation and the results will be intimated to the candidate concerned. Revaluation is permitted only for Theory courses and Theory cum Practical courses where end semester examination is involved.

14. SUPPLEMENTARY EXAMINATION

If a candidate fails to clear all courses in the final semester after the announcement of final end semester examination results, he/she shall be allowed to take up supplementary examinations to be conducted within a reasonable time for the courses of final semester alone, so that he/she gets a chance to complete the programme.

15. AWARD OF LETTER GRADES

Range of % of Total Marks	Letter Grade	Grade Point
91 to 100	O (Outstanding)	10
81 to 90	A+ (Excellent)	9
71 to 80	A (Very Good)	8
61 to 70	B+ (Good)	7
50 to 60	B (Average)	6
Less than 50	RA (Reappear)	0
Satisfactory	SF	0
Withdrawal	W	-
Absent	AB	-
Shortage of Attendance in a course	SA	-

The Grade Point Average (GPA) is calculated using the formula:

$$\text{GPA} = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in the specific semester}}{\sum(\text{course credits}) \text{ for all courses in the specific semester}}$$

The Cumulative Grade Point Average (CGPA) is calculated from first semester (third semester for lateral entry candidates) to final semester using the formula

$$\text{CGPA} = \frac{\sum[(\text{course credits}) \times (\text{grade points})] \text{ for all courses in all the semesters so far}}{\sum(\text{course credits}) \text{ for all courses in all the semesters so far}}$$

The GPA and CGPA are computed only for the candidates with a pass in all the courses.

The GPA and CGPA indicate the academic performance of a candidate at the end of a semester and at the end of successive semesters respectively.

A grade sheet for each semester shall be issued containing Grade obtained in each course, GPA and CGPA.

A duplicate copy, if required can be obtained on payment of a prescribed fee and satisfying other procedure requirements.

Withholding of Grades: The grades of a candidate may be withheld if he/she has not cleared his/her dues or if there is a disciplinary case pending against him/her or for any other reason.

16. ELIGIBILITY FOR THE AWARD OF DEGREE

A candidate shall be declared to be eligible for the award of the ME / MTech Degree provided the candidate has

i. Successfully completed all the courses under the different categories, as specified in the regulations.

ii. Successfully gained the required number of total credits as specified in the curriculum corresponding to the candidate's programme within the stipulated time (vide clause 5).

iii. Successfully passed any additional courses prescribed by the respective Board of Studies whenever readmitted under regulations other than R-2020 (vide clause 11.3)

iv. No disciplinary action pending against him / her.

17. CLASSIFICATION OF THE DEGREE AWARDED

17.1 First Class with Distinction:

17.1.1 A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 8.50

(OR)

17.1.2 A candidate who joins from other institutions on transfer or a candidate who gets readmitted and has to move from one regulation to another regulation and who qualifies for the award of the degree (vide clause 16) and satisfies the following conditions shall be declared to have passed the examination in First class with Distinction:

- Should have passed the examination in all the courses of all the four semesters in the **First Appearance** within four consecutive semesters excluding the authorized break of study (vide clause 11) after the commencement of his / her study.
- Submission of equivalent course list approved by the respective Board of studies.
- Withdrawal from examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 9.00

17.2 First Class:

A candidate who qualifies for the award of the degree (vide clause 16) and who satisfies the following conditions shall be declared to have passed the examination in First class:

- Should have passed the examination in all the courses of all four semesters within six consecutive semesters excluding authorized break of study (vide clause 11) after the commencement of his / her study.
- Withdrawal from the examination (vide clause 10) shall not be considered as an appearance.
- Should have secured a CGPA of not less than 7.00

17.3 Second Class:

All other candidates (not covered in clauses 17.1 and 17.2) who qualify for the award of the degree (vide clause 16) shall be declared to have passed the examination in Second Class.

17.4 A candidate who is absent for end semester examination in a course / project work after having registered for the same shall be considered to have appeared for that examination for the purpose of classification.

18. MALPRACTICES IN TESTS AND EXAMINATIONS

If a candidate indulges in malpractice in any of the tests or end semester examinations, he/she shall be liable for punitive action as per the examination rules prescribed by the college from time to time.

19. AMENDMENTS

Notwithstanding anything contained in this manual, the Kongu Engineering College through the Academic council of the Kongu Engineering College, reserves the right to modify/amend without notice, the Regulations, Curricula, Syllabi, Scheme of Examinations, procedures, requirements, and rules pertaining to its ME / MTech programme.

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CURRICULUM BREAKDOWN STRUCTURE						
Summary of Credit Distribution						
Category	**Semester**				**Total number of credits**	**Curriculum Content (% of total number of credits of the program)**
	I	**II**	**III**	**IV**		
FC(MATHS)	**4**	**-**	**-**	**-**	**4**	**5.55**
PC	**16**	**11**	**3**	**-**	**30**	**41.66**
PE	**3**	**9**	**-**	**6**	**18**	**25.00**
EC		**2**	**9**	**9**	**20**	**27.78**
Semesterwise Total	**23**	**22**	**12**	**15**	**72**	**100.00**

Category	Abbreviation
Lecture hours per week	**L**
Tutorial hours per week	**T**
Practical, Project work, Internship, Professional Skill Training, Industrial Training hours per week	**P**
Credits	**C**

S. No.	Course Code	Course Name	L	T	P	C	Sem
1.	20AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	1
Total Credits to be earned						4	
PROFESSIONAL CORE (PC)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
1.	20GET11	Introduction to Research	2	1	0	3	1
2.	20VLT11	Advanced Digital System Design	3	1	0	4	1
3.	20VLT12	VLSI Design Techniques	3	1	0	4	1
4.	20VLT13	HDL for IC Design	3	0	0	3	1
5.	20VLL11	VLSI Design Laboratory	0	0	2	1	1
6.	20VLL12	HDL for IC Design Laboratory	0	0	2	1	1
7.	20VLT21	Analog Integrated Circuits	3	1	0	4	2
9.	20VLT22	Application Specific Integrated Circuits	3	0	0	3	2
10.	20VLT23	Device Modeling	3	0	0	3	2

11.	20VLT24	VLSI Signal Processing	3	0	0	3	2
12.	20VLL21	Application Specific Integrated Circuits Laboratory	0	0	2	1	2
Total Credits to be earned						30	
PROFESSIONAL ELECTIVE (PE)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
		Elective 1					
1.	20VLE01	Testing of VLSI Circuits	3	0	0	3	1
2.	20VLE02	VLSI Technology	3	0	0	3	1
3.	20VLE03	Semiconductor memory design	3	0	0	3	1
		Elective 2					
4.	20VLE04	Hardware – Software Co-Design	3	0	0	3	2
5.	20VLE05	Computer Aided Design of VLSI Circuits	3	0	0	3	2
6.	20VLE06	Mixed Signal VLSI Design	3	0	0	3	2
		Elective 3					
7.	20VLE07	Low Power VLSI Design	3	0	0	3	2
8.	20VLE08	Electromagnetic Interference and Compatibility	3	0	0	3	2
9.	20VLE09	Reconfigurable Architectures For VLSI	3	0	0	3	2
		Elective 4					
10.	20VLE10	Nature Inspired Optimization Technique	3	0	0	3	3
11.	20VLE11	Supervised Machine Learning Algorithms	3	0	0	3	3
12.	20VLE12	Signal and Image Processing for Real Time Applications	3	0	0	3	3
		Elective 5					
13.	20VLE13	RF Circuit Design	3	0	0	3	4
14.	20VLE14	MEMS Design	3	0	0	3	4
15.	20VLE15	VLSI for IOT Systems	3	0	0	3	4
16.	20VLE16	Quantum Information and Computing	3	0	0	3	4
		Elective 6					
17.	20VLE17	System On Chip	3	0	0	3	4
18.	20VLE18	DSP Processor Architecture and Programming	3	0	0	3	4
19.	20VLE19	Genetic Algorithm for VLSI Design	3	0	0	3	4

20.	20GET13	Innovation, Entrepreneurship and Venture development	3	0	0	3	4
Total Credits to be earned						18	
EMPLOYABILITY ENHANCEMENT COURSES (EC)							
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**C**	**Sem**
1.	20VLP21	Innovative project	0	0	4	2	II
2.	20VLP31	Industrial Project	0	0	18	9	III
3.	20VLP41	Project Work	0	0	18	9	IV
Total Credits to be earned						20	

KEC R2020: SCHEDULING OF COURSES – ME (VLSI Design) Total Credits : 72

Sem	Course1	Course2	Course3	Course4	Course5	Course6	Course7	Course8	Credits
I	20GET11 Introduction to Research (PC-2-1-0-3)	20AMT13 Applied Mathematics for Electronic Engineers (FC-3-1-0-4)	20VLT11 Advanced Digital System Design (PC-3-1-0-4)	20VLT12 VLSI Design Techniques (PC-3-1-0-4)	20VLT13 HDL for IC Design (PC-3-0-0-3)	20VLL11 VLSI Design Laboratory (PC-0-0-2-1)	20VLL12 HDL for IC Design Laboratory (PC-0-0-2-1)	Professional Elective - I (PE-3-0-0-3)	23
II	20VLT21 Analog Integrated Circuits (PC-3-1-0-4)	20VLT22 Application Specific Integrated Circuits (PC-3-0-0-3)	20VLT23 Device Modeling (PC-3-0-0-3)	20VLT24 VLSI Signal Processing (PC-3-0-0-3)	Professional Elective - II (PE-3-0-0-3)	Professional Elective - III (PE-3-0-0-3)	20VLL21 Application Specific Integrated Circuits Laboratory (PC-0-0-2-1)	20VLP21 Innovative Project (EC-0-0-4-2)	22
III	Professional Elective - IV (PE-3-0-0-3)	20VLP31 Industrial Project (EC-0-0-18-9)							12
IV	Professional Elective - V (PE-3-0-0-3)	Professional Elective - VI (PE-3-0-0-3)	20VLP41 Project work (EC-0-0-18-9)						15

MAPPING OF COURSES WITH PROGRAM OUTCOMES

Sem.	Course Code	Course Title	PO1	PO2	PO3	PO4	PO5	PO6
1	20GET11	Introduction to Research	✓	✓	✓	✓	✓	✓
1	20AMT13	Applied Mathematics for Electronics Engineers	✓		✓	✓	✓	✓
1	20VLT11	Advanced Digital System Design	✓	✓	✓	✓	✓	
1	20VLT12	VLSI Design Techniques	✓	✓	✓	✓	✓	
1	20VLT13	HDL for IC Design	✓		✓	✓	✓	✓
1	20VLL11	VLSI Design Laboratory	✓	✓	✓	✓		
1	20VLL12	HDL for IC Design Laboratory	✓	✓	✓	✓		
2	20VLT21	Analog Integrated Circuits	✓		✓	✓	✓	✓
2	20VLT22	Application Specific Integrated Circuits	✓	✓	✓	✓	✓	✓
2	20VLT23	Device Modeling	✓	✓	✓	✓	✓	✓
2	20VLT24	VLSI Signal Processing	✓	✓	✓	✓		
2	20VLL21	Application Specific Integrated Circuits Laboratory	✓	✓	✓	✓		
2	20VLP21	Innovative Project	✓	✓	✓	✓	✓	✓
3	20VLP31	Industrial Project	✓	✓	✓	✓	✓	✓
4	20VLP41	Project Work	✓	✓	✓	✓	✓	✓
		Professional Elective Courses						
1	20VLE01	Testing of VLSI Circuits			✓		✓	
1	20VLE02	VLSI Technology		✓	✓			
1	20VLE03	Semiconductor memory design	✓	✓	✓	✓		

MAPPING OF COURSES WITH PROGRAM OUTCOMES

Sem.	Course Code	Course Title	PO1	PO2	PO3	PO4	PO5	PO6
2	20VLE04	Hardware – Software Co-Design	✓	✓	✓	✓	✓	✓
2	20VLE05	Computer Aided Design of VLSI Circuits	✓	✓	✓	✓	✓	✓
2	20VLE06	Mixed Signal VLSI Design	✓	✓	✓	✓	✓	
2	20VLE07	Low Power VLSI Design	✓	✓	✓	✓	✓	✓
2	20VLE08	Electromagnetic Interference and Compatibility	✓	✓	✓			
2	20VLE09	Reconfigurable Architectures For VLSI	✓		✓	✓	✓	✓
3	20VLE10	Nature Inspired Optimization Technique	✓	✓		✓	✓	
3	20VLE11	Supervised Machine Learning Algorithms	✓	✓	✓		✓	
3	20VLE12	Signal and Image Processing for Real Time Applications	✓		✓	✓		
4	20VLE13	RF Circuit Design	✓		✓	✓		
4	20VLE14	MEMS Design	✓	✓		✓		
4	20VLE15	VLSI for IOT Systems	✓		✓			
4	20VLE16	Quantum Information and Computing	✓		✓			
4	20VLE17	System On Chip	✓		✓			
4	20VLE18	DSP Processor Architecture and Programming	✓	✓	✓	✓		
4	20VLE19	Genetic Algorithm for VLSI Design	✓	✓	✓	✓	✓	✓
4	20GET13	Innovation, Entrepreneurship and Venture development	✓	✓	✓	✓		

M.E. VLSI DESIGN CURRICULUM – R2020

SEMESTER – I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory									
20GET11	Introduction to Research	2	1	0	3	50	50	100	PC
20AMT13	Applied Mathematics for Electronics Engineers	3	1	0	4	50	50	100	FC
20VLT11	Advanced Digital System Design	3	1	0	4	50	50	100	PC
20VLT12	VLSI Design Techniques	3	1	0	4	50	50	100	PC
20VLT13	HDL for IC Design	3	0	0	3	50	50	100	PC
	Professional Elective-I	3	0	0	3	50	50	100	PE
Practical / Employability Enhancement									
20VLL11	VLSI Design Laboratory	0	0	2	1	100	0	100	PC
20VLL12	HDL for IC Design Laboratory	0	0	2	1	100	0	100	PC
	Total Credits to be earned				**23**				

SEMESTER – II

Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory									
20VLT21	Analog Integrated Circuits	3	1	0	4	50	50	100	PC
20VLT22	Application Specific Integrated Circuits	3	0	0	3	50	50	100	PC
20VLT23	Device Modeling	3	0	0	3	50	50	100	PC
20VLT24	VLSI Signal Processing	3	0	0	3	50	50	100	PC
	Professional Elective II	3	0	0	3	50	50	100	PE
	Professional Elective III	3	0	0	3	50	50	100	PE
Practical / Employability Enhancement									
20VLL21	Application Specific Integrated Circuits Laboratory	0	0	2	1	100	0	100	PC
20VLP21	Innovative project	0	0	4	2	50	50	100	EC
Total Credits to be earned					**22**				

SEMESTER – III									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Practical / Employability Enhancement									
	Professional Elective IV	3	0	0	3	50	50	100	PE
20VLP31	Industrial Project	0	0	18	9	50	50	100	EC
Total Credits to be earned					**12**				

SEMESTER – IV									
Course Code	Course Title	Hours / Week			Credit	Maximum Marks			Category
		L	T	P		CA	ESE	Total	
Theory/Theory with Practical									
	Open Elective-I/Professional Elective-V	3	0	0	3	50	50	100	PE
	Open Elective-II/Professional Elective-VI	3	0	0	3	50	50	100	PE
Practical / Employability Enhancement									
20VLP41	Project Work	0	0	18	9	50	50	100	EC
Total Credits to be earned					**15**				

LIST OF PROFESSIONAL ELECTIVES						
Course Code	**Course Title**	**Hours/Week**			**Credit**	**Category**
		L	**T**	**P**		
SEMESTER I						
20VLE01	Testing of VLSI Circuits	3	0	0	3	PE
20VLE02	VLSI Technology	3	0	0	3	PE
20VLE03	Semiconductor memory design	3	0	0	3	PE
SEMESTER II						
20VLE04	Hardware – Software Co-Design	3	0	0	3	PE
20VLE05	Computer Aided Design of VLSI Circuits	3	0	0	3	PE
20VLE06	Mixed Signal VLSI Design	3	0	0	3	PE
20VLE07	Low Power VLSI Design	3	0	0	3	PE
20VLE08	Electromagnetic Interference and Compatibility	3	0	0	3	PE
20VLE09	Reconfigurable Architectures For VLSI	3	0	0	3	PE
20VLE10	Nature Inspired Optimization Technique	3	0	0	3	PE
20VLE11	Supervised Machine Learning Algorithms	3	0	0	3	PE
20VLE12	Signal and Image Processing for Real Time Applications	3	0	0	3	PE
SEMESTER IV - LIST OF PROFESSIONAL/ OPEN ELECTIVES						
20VLE13	RF Circuit Design	3	0	0	3	PE
20VLE14	MEMS Design	3	0	0	3	PE
20VLE15	VLSI for IOT Systems	3	0	0	3	PE
20VLE16	Quantum Information and Computing	3	0	0	3	PE
20VLE17	System On Chip	3	0	0	3	PE
20VLE18	DSP Processor Architecture and Programming	3	0	0	3	PE
20VLE19	Genetic Algorithm for VLSI Design	3	0	0	3	PE
20GET13	Innovation, Entrepreneurship and Venture development	3	0	0	3	PE

20GET11 INTRODUCTION TO RESEARCH

(Common to Engineering and Technology Branches)

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	I	PC	2	1	0	3

Preamble	This course will familiarize the fundamental concepts/techniques adopted in research, problem formulation and patenting. Also will disseminate the process involved in collection, consolidation of published literature and rewriting them in a presentable form using latest tools.	
Unit - I	**Concept of Research:**	**9**
Meaning and Significance of Research: Skills, Habits and Attitudes for Research - Time Management - Status of Research in India. Why, How and What a Research is? - Types and Process of Research - Outcome of Research - Sources of Research Problem - Characteristics of a Good Research Problem - Errors in Selecting a Research Problem - Importance of Keywords - Literature Collection – Analysis - Citation Study - Gap Analysis - Problem Formulation Techniques.		
Unit - II	**Research Methods and Journals:**	**9**
Interdisciplinary Research - Need for Experimental Investigations - Data Collection Methods - Appropriate Choice of Algorithms / Methodologies / Methods - Measurement and Result Analysis - Investigation of Solutions for Research Problem - Interpretation - Research Limitations. Journals in Science/Engineering - Indexing and Impact factor of Journals - Citations - h Index - i10 Index - Journal Policies - How to Read a Published Paper - Ethical issues Related to Publishing - Plagiarism and Self-Plagiarism.		
Unit - III	**Paper Writing and Research Tools:**	**9**
Types of Research Papers - Original Article/Review Paper/Short Communication/Case Study - When and Where to Publish? - Journal Selection Methods. Layout of a Research Paper - Guidelines for Submitting the Research Paper - Review Process - Addressing Reviewer Comments. Use of tools / Techniques for Research - Hands on Training related to Reference Management Software - EndNote, Software for Paper Formatting like LaTeX/MS Office. Introduction to Origin, SPSS, ANOVA etc., Software for detection of Plagiarism.		
Unit - IV	**Effective Technical Thesis Writing/Presentation:**	**9**
How to Write a Report - Language and Style - Format of Project Report - Use of Quotations - Method of Transcription Special Elements: Title Page - Abstract - Table of Contents - Headings and Sub-Headings - Footnotes - Tables and Figures - Appendix - Bibliography etc. - Different Reference Formats. Presentation using PPTs.		
Unit - V	**Nature of Intellectual Property:**	**9**
Patents - Designs - Trade and Copyright. Process of Patenting and Development: Technological research - innovation - patenting - development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents.		

Total:45

REFERENCES:

1	DePoy, Elizabeth, and Laura N. Gitlin, “Introduction to Research-E-Book: Understanding and Applying Multiple Strategies”, Elsevier Health Sciences, 2015.
2	Walliman, Nicholas, “Research Methods: The basics”, Routledge, 2017.
3	Bettig Ronald V., “Copyrighting culture: The political economy of intellectual property”, Routledge, 2018.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	list the various stages in research and categorize the quality of journals.	Analyzing (K4)
CO2	formulate a research problem from published literature/journal papers	Evaluating (K5)
CO3	write, present a journal paper/ project report in proper format	Creating (K6)
CO4	select suitable journal and submit a research paper.	Applying (K3)
CO5	compile a research report and the presentation	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	1			
CO2	3	2	3			
CO3	3	3	1			
CO4	3	2	1			
CO5						

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

20AMT13 APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS

(Common to VLSI Design and Embedded Systems)

Programme & Branch	M.E.- VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	NIL	I	FC	3	1	0	4

Preamble	This course will demonstrate various analytical skills in applied mathematics and use extensive mathematical tools such as linear programming, matrix factorizations and queuing theory with the tactics of problem solving and logical thinking applicable in electronics engineering.	
Unit - I	**Advanced Matrix Theory**:	**9+3**
Positive definite matrices – Cholesky decomposition – Generalized Eigenvectors – Canonical basis – QR factorization – Generalized inverses – Singular value decomposition – Least squares solution.		
Unit - II	**Vector Spaces:**	**9+3**
Definition – Subspaces – Linear dependence and independence – Basis and dimension – Row space, Column space and Null Space – Rank and nullity.		
Unit - III	**Linear Programming:**	**9+3**
Mathematical Formulation of LPP – Basic definitions – Solutions of LPP: Graphical method – Simplex method – Transportation Model – Mathematical Formulation – Initial Basic Feasible Solution: North west corner rule – Vogel's approximation method – Optimum solution by MODI method – Assignment Model – Mathematical Formulation – Hungarian algorithm.		
Unit - IV	**Non-Linear Programming**	**9+3**
Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables.		
Unit - V	**Queuing Theory:**	**9+3**
Markovian queues – Single and Multi-server Models – Little's formula – Non- Markovian Queues – Pollaczek Khintchine Formula.		

Lecture:45, Practical:15, Total:60

REFERENCES:

1	Bronson, R., "Matrix Operations", Schaum's Outline Series, McGraw Hill, 2011.
2	Howard Anton, "Elementary Linear Algebra" 10th edition, John Wiley & Sons, 2010.
3	Kanti Swarup, Gupta, P.K and Man Mohan "Operations Research", S.Chand & Co., 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	apply various methods in matrix theory to solve system of linear equations.	Applying (K3)
CO2	apply the concepts of linear algebra to solve practical problems.	Applying (K3)
CO3	formulate mathematical models for linear programming problems and solve the transportation and assignment problems.	Applying (K3)
CO4	use non-linear programming concepts in real life situations.	Applying (K3)
CO5	identify the suitable queuing model to handle communication problems.	Applying (K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3					
CO2	3					
CO3	3				2	
CO4	3		3	3	2	
CO5	3			3		

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	20	70	-	-	-	100
CAT2	10	20	70	-	-	-	100
CAT3	10	20	70	-	-	-	100
ESE	10	20	70	-	-	-	100

*** +3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20VLT11 ADVANCED DIGITAL SYSTEM DESIGN

(Common to VLSI Design and Embedded Systems)

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	I	PC	3	1	0	4

Preamble	To design and analyze synchronous, asynchronous digital circuits and to introduce ASM and the architectures of PLD	
Unit - I	**Synchronous Sequential Circuit Design:**	**9**
Analysis of Clocked Synchronous Sequential Networks (CSSN)- Modeling of CSSN – State table Reduction- Stable Assignment – Complete Design of CSSN – Design of Iterative Circuits		
Unit - II	**Algorithmic State Machine(ASM):**	**9**
ASM-ASM Chart – Synchronous Sequential Network Design Using ASM Charts- State Assignment- ASM Tables-ASM Realization- Asynchronous Inputs.		
Unit - III	**Asynchronous Circuit Design:**	**9**
Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards		
Unit - IV	**Programming Logic Arrays:**	**9**
PLA minimization – Essential Prime Cube theorem- PLA folding- foldable compatibility matrix- The Compact Algorithm. Practical PLA's –Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.		
Unit - V	**Programmable Devices:**	**9**
Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL – Realization State machine using PLD – Complex Programmable Logic Devices (CPLDs) – FPGA – Actel ACT.		

Lecture: 45, Tutorial :15,Total: 60

REFERENCES:

1.	Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2008
2.	Biswas Nripendra N, "Logic Design Theory", Prentice Hall of India, New Delhi, 2001
3	Yarbrough, John M., "Digital Logic Applications and Design", Thomson Learning, Singapore, 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design clocked synchronous sequential circuits using state table reduction and assignment	Applying(K3)
CO2	realize the algorithmic state machine using state tables, charts and state assignment	Applying(K3)
CO3	analyze the asynchronous sequential circuit using flow table reduction and find the hazards in circuits	Analyzing(K4)
CO4	simplify the circuits using Programmable logic array, essential cube theorem and compact algorithm	Applying(K3)
CO5	design the synchronous sequential circuits using Programmable Logic Device, Programmable Array Logic and CPLD	Creating(K6)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3	2		3	
CO2	3	3	2		2	
CO3	3	3	2	1	3	
CO4	3	3	2	1	3	
CO5	3	3	2	1	3	

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	5	15	80				100
CAT2	5	15	70	10			100
CAT3		10	60	20		10	100
ESE	5	15	55	15		10	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20VLT12 VLSI DESIGN TECHNIQUES

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	I	PC	3	1	0	4

Preamble	To design the various combinational circuits and sequential circuits using VLSI Design Techniques	
Unit - I	**Overview of VLSI Design Methodologies:**	**9+3**
VLSI Design Flow-Design Hierarchy-VLSI Design Styles-Review of Fabrication process-CMOS n-well process & SOI process-Layout Design Rules-Review of MOS Transistor Theory: Structure, Operation-MOSFET Current-Voltage Characteristics-Threshold Voltage-MOSFET Capacitances		
Unit - II	**MOS Inverters Characteristics:**	**9+3**
Static:-Resistive –Load Inverter-Inverters with MOSFET Load-CMOS Inverter. Switching: Delay Time definitions-Calculation of delay times-Inverter Design with Delay constraints- Power Delay product and Energy delay product.		
Unit - III	**Logic Design:**	**9+3**
CMOS Static& Complementary logic-CMOS Transmission Gates-Pass Transistor Circuit-Synchronous Dynamic Circuit-Dynamic CMOS Circuit Techniques-High performance CMOS Circuits.		
Unit - IV	**Sequential MOS Logic Circuits:**	**9+3**
Behavior of Bistable Elements-Latch Circuit-Flipflop Circuits-CMOS D Latch and Edge triggered Flipflop-Sense Amplifier based Flipflops.		
Unit - V	**VLSI Building Block Design:**	**9+3**
Arithmetic Building Block-Adders, Multipliers, Shifters, On chip Clock generation and Distribution-Memory Design.		

Lecture:45, Tutorial:15, Total:60

REFERENCES:

1	Sung-Mokang, Yusuf Leblebici, Chulwoo Kim “CMOS Digital Integrated Circuits Analysis and Design”, McGraw Hill, Fourth Edition, 2016.
2	Jan M Rabaey, “Digital Integrated Circuits", Prentice Hall, 2004.
3	Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, Third edition, 2007.

COURSE OUTCOMES: On completion of the course, the students will be able to	**BT Mapped (Highest Level)**

CO1	infer the steps in different fabrication methodologies	Understanding(K2)
CO2	apply design rules and generate layout	Applying(K3)
CO3	analyze CMOS inverter with delay constraints	Analyzing(K4)
CO4	design Combinational and sequential circuits	Creating(K6)
CO5	analyze Adders, Multipliers, Shifters and Memory	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3			
CO2				2	3	
CO3			2	2	3	
CO4			2	2	3	
CO5			2	2	3	

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	60	30	-	-	-	100
CAT2	10	40	35	15	-	-	100
CAT3	10	45	35	-	-	10	100
ESE	10	40	30	10	-	10	100

*** ±3% may be varied**

20VLT13 HDL for IC Design

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit

Prerequisites	Nil	I	PC	3	0	0	3

Preamble	To design and implement digital logic circuits using verilog in FPGA and to verify the functionality using Blue Spec.	
Unit - I	**Introduction to Verilog:**	**9**
Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Basic Concepts-Gate level Modeling-Dataflow Modeling-Behaviour Modeling-Tasks and Functions-Switch level modeling.		
Unit - II	**Design using Verilog:**	**9**
Logic Synthesis using verilog HDL: Verilog HDL Synthesis-Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis.		
Unit - III	**Introduction to Bluespec System Verilog:**	**9**
Building the design-Multiple modules in a single package-Multiple package in single design-Data types-Variables-assignments-combinational circuits.		
Unit - IV	**Modeling usingBluespec System Verilog:**	**9**
Modelling Rules, registers, and FIFOs-Module hierarchy and interfaces-Scheduling-RWires and Wire types- Polymorphism- Advanced types and pattern.		
Unit - V	**System Design Using Bluespec System Verilog:**	**9**
Matching-Static elaboration - For-loops/while-loops-Expressions-Vectors-Finite State Machines (FSMs)-Importing existing RTL into a BSV design.		

Lecture:45, Total:45

REFERENCES:

1	Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education New Delhi, 2003.
2	Chris Spear System Verilog for Verification: “A Guide to Learning the Test bench Language Features”, 2nd Edition, Springer, 2012.
3	https://ocw.mit.edu – Massachusetts Institute of Technology Open Courseware

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	apply digital design concepts and write Verilog programs for the design.	Applying(K3)
CO2	synthesis the digital circuit and implement in FPGA	Evaluating(K4)

CO3	comprehend the basics of system design using Bluespec System Verilog	Understanding(K2)
CO4	model systems using Bluespec System Verilog	Evaluating(K5)
CO5	developsystems using FSM	Creating(K6)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3		3	
CO2	3		3	3	3	
CO3	2		3			3
CO4			3		3	
CO5	3		3	3		3

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1		30	60	10			100
CAT2	10	30	60				100
CAT3	10	30	60				100
ESE	10	30	50	10			100

*** ±3% may be varied**

20VLL11 VLSI DESIGN LABORATORY

Programme & Branch	M.E-VLSI Design	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	I	PC	0	0	2	1
Preamble	To impart the knowledge of design and layout of digital circuits						

List of Exercises / Experiments :

1.	Layout Design for basic logic gates
2.	Design and Analysis of CMOS Inverter
3.	Sequential circuit design-I
4.	Sequential circuit design-II
5.	Design of Adders
6.	Design of Multipliers
7.	Design of Shifters
8.	Design of Memory Design
9.	Logic design using pass transistor and transmission gates
10.	Multiplexer

Practical : 30,Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	Laboratory Manual
2.	Cadence- Virtuoso

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design Digital systems at transistor level	Applying(K3), Precision(S3)
CO2	obtain the layout of digital systems	Applying (K3), Precision (S3)
CO3	analyse the characteristics of digital Circuits	Analyzing (K4), Precision(S3)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	1	1		
CO2	3	2	1	1		
CO3	3	2	1	1		
CO4						
CO5						
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

20VLL12 HDL FOR IC DESIGN LABORATORY

Programme & Branch	**M.E-VLSI Design**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**I**	**PC**	**0**	**0**	**2**	**1**
Preamble	To impart the knowledge of design and implementation of digital circuits using VHDL and Verilog Hardware						

	Description Language

List of Exercises / Experiments :

1.	Modeling of Sequential Digital Systems with Test benches
2.	State Machine Design
3.	Memory Design
4.	Design and implementation of ALU, MAC using FPGA
5.	Design and implementation of different adders using FPGA
6.	Design and implementation of pipelined array multiplier using FPGA
7.	Modeling Combinational circuits using Bluespec System verilog
8.	FIFO design using Bluespec system verilog
9.	Design on FSM using Bluespec system verilog

Practical : 30,Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	Laboratory Manual
2.	Modelsim
3.	Xilinx

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	design Digital systems using Verilog and Verilog	Applying(K3), Precision(S3)
CO2	implement Digital systems in FPGA	Applying (K3), Precision (S3)
CO3	design digital Circuits using Bluespec	Applying (K3), Precision(S3)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	1	1		
CO2	3	2	1	1		
CO3	3	2	1	1		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

20VLT21 ANALOG INTEGRATED CIRCUITS

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**II**	**PC**	**3**	**1**	**0**	**4**

Preamble	To focus on the concepts of MOSFETs and design of differential amplifiers, feedback amplifiers and their stability with

	practical knowledge .	
Unit - I	**Basic MOS Device Physics and Single Stage Amplifiers:**	**9+3**
Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models- Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.		
Unit - II	**Differential Amplifiers and Current Mirrors:**	**9+3**
Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common-Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors.		
Unit - III	**Frequency Response of Amplifiers and Noise:**	**9+3**
Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.		
Unit - IV	**Feedback and Operational Amplifiers:**	**9+3**
Feedback Amplifiers- General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common– Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps.		
Unit - V	**Stability and Frequency Compensation:**	**9+3**
General Considerations-Multipole Systems- Phase Margin-Frequency Compensation-Compensating of Two-Stage Op Amps-Other Compensation Techniques.		

Lecture:45, Tutorial:15, Total:60

REFERENCES:

1	B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill Edition 2002.
2	Paul. R.Gray, Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, (4/e),2001.
3	D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, Wiley, 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts of MOS Devices physics, Single stage amplifiers, Differential Amplifiers and Current Mirrors	Understanding(K2)
CO2	analyze single stage amplifiers, Differential Amplifier and Current Mirror	Analyzing(K4)

CO3	examine the frequency response of amplifiers and the effects of noise in amplifiers	Analyzing(K4)
CO4	design feedback and operational amplifiers	Creating(K6)
CO5	appreciate the frequency compensation techniques	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3		3	3	3	3
CO2	3		3	3	3	3
CO3	3		3	3	3	3
CO4	3		3	3	3	3
CO5	3		3	3		3

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	40	30	10			100
CAT2	40	10	20	30			100
CAT3	20	40	20	20			100
ESE	20	30	30	20			100

*** ±3% may be varied**

20VLT22 APPLICATION SPECIFIC INTEGRATED CIRCUITS

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	VLSI Design Techniques	II	PC	3	0	0	3

Preamble	To know the different programmable ASICs, logic cells, I/O cells and interconnect and to learn how synthesis and

	physical design flow in carried out in an ASIC design.	
Unit - I	**Introduction to ASICs, CMOS Logic and ASIC Library Design:**	**9**
Types of ASICs - Design flow - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort.		
Unit - II	**Programmable ASICs, Programmable ASIC Logic Cells And Programmable ASIC I/O Cells:**	**9**
Anti fuse - static RAM - EPROM and EEPROM technology - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.		
Unit - III	**Programmable ASIC Interconnect:**	**9**
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX.		
Unit - IV	**Design and synthesis:**	**9**
Design systems - Half gate ASIC –Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation-.Logic synthesis – Logic Simulation - Design and synthesis of various circuits.		
Unit - V	**Physical Design:**	**9**
ASIC Partitioning - floor planning- placement and routing – power and clocking strategies - DRC..		

Lecture:45, Total:45

REFERENCES:

1	M.J.S.Smith, " Application - Specific Integrated Circuits", Pearson,2003
2	Steve Kilts, “Advanced FPGA Design,” Wiley Inter-Science
3	Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementation of Signal Processing Systems”, Wiley, 2008

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	demonstrate ASIC Design flow and comprehend the types of ASIC	Understanding(K2)
CO2	realize the issues involved in ASIC design, including design, role of transistor, logical effort and programming technology	Understanding(K2)
CO3	analyze the issues involved in logic cells, I/O cells and interconnect	Analysing(K3)
CO4	perform simulation and synthesis of the design using different programmable ASIC design software	Applying(K3)
CO5	analyze the algorithms used in partitioning, Floorplanning , placement,routing, power and clock design for ASIC	Analyzing(K4)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3			
CO2	2		3			
CO3	2		3	2	2	
CO4	3		3	3	3	3
CO5	3	2	3	3	3	
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	35	45				100
CAT2	15	35	30	20			100
CAT3	20	20	30	30			100
ESE	15	35	30	20			100

*** ±3% may be varied**

20VLT23 DEVICE MODELING

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**II**	**PC**	**3**	**0**	**0**	**3**

Preamble	To analyze the solid state devices using mathematical concepts	
Unit - I	**Semiconductor Physics and Modeling of Passive Devices:**	**9**
Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion- Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects-Modeling of resistors-Modeling of Capacitors-		

Modeling of Inductors.		
Unit - II	**Diode and Bipolar Device Modeling :**	**9**
Abrupt and linear graded PN junction- Ideal diode current equation- Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters Transistor Action-Terminal currents -Switching- Static, Small signal and Large signal Eber-Moll models of BJT- temperature and area effects.		
Unit - III	**MOSFET Modeling and Parameter Measurements:**	**9**
MOS Transistor – NMOS- PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect- Models for MOSFET.		
Unit - IV	**Noise Models and BSIM4 MOSFET Model:**	**9**
Noise Sources in MOSFET-Flicker Noise Modeling-Thermal Noise Modeling- BSIM4 MOSFET Model-Gate Dielectric Model-Enhanced Models for Effective DC and AC Channel Length and width-Threshold Voltage Model-I-V Model.		
Unit - V	**Other MOSFET Models:**	**9**
EKV Model-Model Features-Long Channel Drain Current Model-Modeling Second order Effects of Drain Current-Effect of Charge Sharing-Modeling of Charge storage Effects-Non-quasi static Modeling-Noise Models-Temperature Effects-MOS Model 9-MOSAI Model.		

Lecture: 45,Total: 45

REFERENCES:

1.	Massobrio Giuseppe and Antognetti Paolo, “Semiconductor Device Modeling with SPICE”, Second Edition, McGraw-Hill Inc, New York, 2010
2.	Sze S. M., “Semiconductor Devices-Physics and Technology”, 2nd Edition, John Wiley and Sons, New York, 2009.
3.	TrondYtterdal,Yuhua Cheng and Tor A.Fjeldly,,”Device Modeling for Analog and RF CMOS Circuit Design”John Wiley &Sons Ltd ,2003.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	realize the concepts of semiconductor physics	Understanding(K2)
CO2	apply mathematical concepts to model basic semiconductor devices	Applying(K3)
CO3	analyse the secondary effects of semiconductor physics using mathematical expressions.	Analyzing(K4)
CO4	analyse the effects of temperature and Area on the performance of semiconductor devices	Analyzing(K4)

CO5	create models for MOSFETs.	Creating(K6)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2		3			2
CO2					3	
CO3		2	3	3	3	
CO4			3	3	2	
CO5	3	3		3	3	

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	10	20	25	25	10	10	100
CAT2	10	20	25	25	10	10	100
CAT3	10	20	25	25	10	10	100
ESE	10	20	25	25	10	10	100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20VLE24 VLSI SIGNAL PROCESSING

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**II**	**PC**	**3**	**0**	**0**	**3**

Preamble	To apply the concepts of VLSI techniques to real time signal processing	
Unit - I	**Introduction to DSP Systems:**	**9**
Introduction To DSP Systems -Typical DSP algorithms; **Iteration Bound** – data flow graph representations, loop bound and iteration		

bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs.**Pipelining and parallel processing:** Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power		
Unit - II	**Retiming & Unfolding:**	**9**
Retiming : Definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. **Unfolding**: Algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application		
Unit - III	**Systolic Architecture Design & Bit Level Arithmetic Architectures:**	**9**
Systolic Architecture Design: Design methodology, FIR systolic arrays **Bit Level Arithmetic Architectures**: Parallel Multipliers, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic		
Unit - IV	**Fast Convolution , Algorithmic strength reduction & Pipelined and Parallel Recursive filters Adaptive Filters**	**9**
Fast Convolution: Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm **Algorithmic strength reduction:** Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT **Pipelined and Parallel Recursive filters Adaptive Filters:**– Pipelining in first- order IIR filters, Parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters		
Unit - V	**Scaling, Round off Noise, Lattice Structure & Numerical Strength Reduction**	**9**
Scaling, Round off Noise: Scaling and Round off Noise- State variable Description of digital filters, Scaling and round off noise computation, Round off noise in pipelined I order IIR filters **Lattice Structure:** Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter **Numerical Strength Reduction**-Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.		

Lecture:45,Total:45

REFERENCES:

1	Parhi, Keshab K., "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Inter Science, New York, 2010
2	Isamail, Mohammed and Fiez, Terri, "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 1994**.**
3	Magdy A. Bayoumi, Magdy A. Bayoumi, E. Swartzlander, "VLSI Signal Processing Technology",Kluwer Academic Publishers.October 1994

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	compute the iteration bound of a circuit	Applying(K3)
CO2	perform pipelining and parallel processing in FIR systems to achieve high speed and low power	Applying(K3)
CO3	improve the speed of digital system through transformation techniques.	Applying(K3)
CO4	apply systolic and bit level architectures to improve the efficiency of VLSI circuits	Applying(K3)

CO5	use of proper techniques for parallel processing design for scaling and roundoff noise computation	Applying(K3)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	3	2			
CO2	3	3	2	3		
CO3	2	3		3		
CO4	3	3	2	3		
CO5	2	3		2		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	15	70				100
CAT2	22	13	65				100
CAT3	10	20	70				100
ESE	15	15	70				100

*** ±3% may be varied**

20VLL21 APPLICATION SPECIFIC INTEGRATED CIRCUITS LABORATORY

Programme & Branch	**M.E-VLSI Design**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**II**	**PC**	**0**	**0**	**2**	**1**
Preamble	To impart the knowledge of physical design of digital circuits and analyse the frequency response of analog circuits						

List of Exercises / Experiments :

1.	Design, simulation and synthesis of Adders

2.	Design, simulation and synthesis of multipliers
3.	Design, simulation and synthesis of memory
4.	Design, simulation and synthesis of Finite state machine
5.	Design, simulation and synthesis of ALU
6.	Complete the design of two differential amplifiers, one of which uses emitter resistor (R_E) biasing, and one ofwhich uses current mirror biasing.
7.	Analysis of frequency response of current series and current shunt feedback topologies.
8.	Analysis of frequency response of voltage series and voltage shunt feedback topologies.
9.	Floor Planning, Routing and Placement procedures-
10.	Analysis of Circuits - Power Planning, Layout generation, LVS and Back annotation, Total power estimation

Practical : 30,Total: 30

REFERENCES/MANUAL/SOFTWARE:

1.	Laboratory Manual
2.	Cadence

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	perform physical design of digital circuits	Applying(K3), Precision(S3)
CO2	analyze the performance of digital systems	Analyzing (K4), Precision (S3)
CO3	analyse the frequency response of analog circuits	Analyzing (K4), Precision(S3)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3	2	1	1		
CO2	3	2	1	1		
CO3	3	2	1	1		
CO4						
CO5						
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

20VLE01 TESTING OF VLSI CIRCUITS

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**I**	**PE**	**3**	**0**	**0**	**3**

Preamble	To know the basics of VLSI test concepts, Test generation, DFT architectures, Built in Self Test and fault diagnosis.	
Unit - I	**Basics of Testing And Fault Modeling:**	**9**

Importance of Testing – Challenges in VLSI testing – Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation		
Unit - II	**Design for Testability:**	**9**
Testability analysis -SCOAP Testability Analysis- Probability-Based Testability Analysis - Design for Testability- *Ad Hoc* Approach- Structured Approach - Scan Cell Designs- Scan Architectures - Scan Design Rules		
Unit - III	**Test Generation for Combinational and Sequential Circuits:**	**9**
Random Test generation- Boolean difference method- ATPG for Combinational Circuits- A Basic ATPG Algorithm- D Algorithm- PODEM- FAN- Designing a Sequential ATPG - Time Frame Expansion - 5-Valued Algebra- Designing a Simulation-Based ATPG.		
Unit - IV	**Self-Test and Test Algorithms:**	**9**
Built-In Self Test - Test pattern generation for BIST - BIST Architectures – RAM Functional Fault Models- RAM Functional Fault Models- Functional Test Patterns and Algorithms- March Tests		
Unit - V	**Fault Diagnosis:**	**9**
Logic Level Diagnosis – Fault Dictionary- Diagnosis by UUT reduction - Fault Diagnosis for Combinational Circuits – Effect cause Analysis- Self-checking design.		

Lecture:45,Total:45

REFERENCES:

1	M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2	Laung – Terng wang, Cheng – wen wu, Xidogingwen, “VLSI Testing Principles andArchitectures: Design for Testability”, Morgan Kaufmann Publisher, 2006
3	M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits", Kluwer Academic Publishers, 2002.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	distinguish between different fault models and types of simulation	Understanding(K2)
CO2	identify the design for testability techniques for combinational and sequential circuits	Applying(K3)
CO3	identify the various test generation methods for combinational and sequential circuits	Applying(K3)
CO4	nderstand the various Built In Self Test architectures, memory fault models and testing of memories	Applying(K3)
CO5	review the various fault diagnosis approach for VLSI Systems	Understanding(K2)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1			3			
CO2			3		3	
CO3			3		3	
CO4			3			
CO5			3			
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	45	40	-	-	-	100
CAT2	10	45	45	-	-	-	100
CAT3	15	45	35	-	-	-	100
ESE	20	40	40	-	-	-	100

*** ±3% may be varied**

20VLE02 VLSI TECHNOLOGY

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**I**	**PE**	**3**	**0**	**0**	**3**

Preamble	To infer the foundations in MOS and CMOS fabrication process..	
Unit - I	**Crystal growth, wafer preparation, Epitaxy and Oxidation:**	**9**
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.		
Unit - II	**Lithography And Relative Plasma Etching:**	**9**

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments.		
Unit - III	**Deposition and Diffusion:**	**9**
Deposition process, Polysilicon, Silicon Dioxide- Silicon Nitride- plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques		
Unit - IV	**Ion implementation and Metallization:**	**9**
Range theory- Implant equipment. Annealing-Shallow junction – High energy implantation – Metallization Applications- Metallization choices- Physical vapor deposition – Patterning.		
Unit - V	**VLSI Process Integration and Packaging of VLSI Devices:**	**9**
NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology – Bipolar IC Technology – IC Fabrication. Package types– banking design consideration – VLSI assembly technology – Package fabrication technology		

Lecture:45,Total:45

REFERENCES:

1	Sze, S.M., "VLSI Technology", Second Edition, McGraw-Hill, New York, 1998.
2	Mukherjee, Amar., "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall India, New Delhi, 2000.
3	Plummer, James D., Deal, Michael D. and Griffin, Peter B., "Silicon VLSI Technology: Fundamentals Practice and Modeling", Prentice Hall India, New Delhi, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	summarize the approach for wafer preparation, Epitaxy and Oxidation	Understanding(K2)
CO2	distinguish the various methods for lithography and plasma etching	Understanding(K2)
CO3	illustrate the various Deposition and diffusion process	Understanding(K2)
CO4	infer the process of ion implantation and metallization	Understanding(K2)
CO5	realize the various IC technology and Package types.	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3			

CO2			3			
CO3			3			
CO4			3			
CO5		2	3			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	47	53					100
CAT2	30	70					100
CAT3	27	73					100
ESE	40	60					100

*** ±3% may be varied**

20VLE03 SEMICONDUCTOR MEMORY DESIGN

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	**Nil**	**I**	**PE**	**3**	**0**	**0**	**3**

Preamble	To study the architectures for SRAM and DRAM, various non-volatile memories, fault modeling and testing of memories for fault detection and the radiation hardening process and issues for memory.	
Unit - I	**Random Access Memory Technologies:**	**9**
SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation- Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology- Advanced SRAM Architectures and Technologies-Application Specific SRAMs DRAM Technology Development- CMOS DRAMs- DRAMs Cell Theory and Advanced Cell Structures- BiCMOS, DRAMs- Soft Error Failures in DRAMs- Advanced DRAM Designs and Architecture- Application Specific DRAMs.		
Unit - II	**Nonvolatile Memories:**	**9**

Masked Read-Only Memories (ROMs)- High Density ROMs- Programmable Read-Only Memories (PROMs)- Bipolar PROMs- CMOS PROMs- Erasable(UV) Programmable Road-Only Memories (EPROMs)- Floating-Gate PROM Cell- One-Time Programmable (OTP) EPROMS- Electrically Erasable PROMs (EEPROMs)- EEPROM Technology and Architecture- Nonvolatile SRAM- Flash Memories (EPROMs or EEPROM)- Advanced Flash Memory Architecture.		
Unit - III	**Memory Fault Modeling And Testing:**	**9**
RAM Fault Modeling, Electrical Testing, Peusdo Random Testing- Megabit DRAM Testing- Nonvolatile Memory Modeling and Testing- IDDQ Fault Modeling and Testing- Application Specific Memory Testing.		
Unit - IV	**Semiconductor Memory Reliability:**	**9**
General Reliability Issues- RAM Failure Modes and Mechanism- Nonvolatile Memory Reliability- Reliability Modeling and Failure Rate Prediction- Design for Reliability- Reliability Test Structures- Reliability Screening and Qualification.		
Unit - V	**Packaging Technologies:**	**9**
Radiation Effects- Single Event Phenomenon (SEP)- Radiation Hardening Techniques- Radiation Hardening Process and Design Issues- Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)- Gallium Arsenide (GaAs) FRAMs- Analog Memories- Magnetoresistive Random Access Memories (MRAMs)- Experimental Memory Devices. Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards- High Density Memory Packaging Future Directions.		

Lecture:45,Total:45

REFERENCES:

1	Sharma, Ashok K., “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press, New York, 2002.
2	Sharma, Ashok K., “Semiconductor Memories”, Two-Volume Set, Wiley-IEEE Press, New York, 2003.
3	Sharma, Ashok K., “Semiconductor Memories: Technology, Testing, and Reliability”, Prentice Hall of India, New Delhi, 1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the micro level operations of Random Access Memories	Understanding(K2)
CO2	analyze the need of non-volatile memories and their applications	Analyzing(K4)
CO3	design the fault free memory systems by fault modeling techniques	Evaluating(K5)
CO4	analyze and design the memory architectures by considering the radiation effects	Analyzing(K4)
CO5	identify the packages for memories	Understanding(K2)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	2	3	2			
CO2	3	3	2	3		
CO3	2	3		3		
CO4	3	3	2	3		
CO5	2	3		2		
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	25	75					100
CAT2	20	50	30				100
CAT3	20	40	25	10	5		100
ESE	20	40	25	10	5		100

*** ±3% may be varied**

20VLE04 HARDWARE SOFTWARE CO-DESIGN

Programme & Branch	**M.E.- VLSI Design**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	NIL	**II**	**PE**	**3**	**0**	**0**	**3**

Preamble	develop an integrated application development environment of hardware/software codesign of embedded system	
Unit - I	**Design Consideration:**	**9**
Platform-Based Design – System Modeling – Video Coding – Image Processing – Cryptography - Digital Communication**.**		
Unit - II	**System Level Design:**	**9**
Abstraction Levels – Algorithm Level Verification – Transaction Level Modeling – System Level Development Tools.		

Unit - III	**Embedded Processor Design:**	**9**
Specific Instruction-Set - Data Level Parallelism – Instruction Level Parallelism – Thread Level Parallelism		
Unit - IV	**Parallel Compiler:**	**9**
Vectorization - SIMDization – ILP Scheduling – Threading - Compiler Technique – Compiler Infrastructures		
Unit - V	**Testing:**	**9**
Real-Time Operating System for PLX: PRRP Scheduler - Memory Management – Communication and Synchronization Primitives - Multimedia Applications in RTOS for PLX – Application Development Environment.		

Lecture: 45, Total: 45

REFERENCES:

1.	Sao-jie Chen , Guang - Huei Lin, Pao -Ann Hsiung and Yu-Hen Hu, "Hardware Software Co-Design of a Multimedia SOC Platform" Springer, 2009.
2.	Jorgen Staunstrup, Wayne Wolf, ”Hardware/Software Co-Design: Principles and Practice” , Kluwer Academic Pub, 1997.
3	Patrick Schaumont, A Practical Introduction to Hardware/Software Codesign, 2nd Edition, Springer, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	acquire knowledge about system level modeling and image and video encoding	Understanding(K2)
CO2	perform algorithm level verification and learn system development tools	Applying(K3)
CO3	distinguish between different levels of parallelism	Applying(K3)
CO4	infer scheduling and compiler techniques	Understanding(K2)
CO5	interpret the requirements of Real time Operating Systems and analyze the integrated application development environment of hardware/software codesign of embedded system	Analyzing(K4)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1	3					
CO2			3		2	
CO3	1	3				
CO4	3					
CO5				2		3
1 – Slight, 2 – Moderate, 3 – Substantial, BT- Bloom's Taxonomy						

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	70					100
CAT2	30	40	30				100
CAT3	30	30	30	10			100
ESE	30	30	30	10			100

*** ±3% may be varied (CAT 1,2,3 – 50 marks & ESE – 100 marks)**

20VLE05 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**ASIC Design**	**II**	**PE**	**3**	**0**	**0**	**3**

Preamble	To give an overview of the VLSI physical design and understand CAD algorithms used in VLSI physical design automation field.	
Unit - I	**Design Methodologies:**	**9**
Introduction to VLSI Design methodologies – Review of VLSI Design automation tools –Algorithmic Graph Theory and Computational Complexity –Tractable and Intractable problems – general purpose methods for combinatorial optimization problems		
Unit - II	**Partitioning, Placement and Floor planning :**	**9**

Placement and Partitioning –Circuit representation – Placement algorithms – Partitioning- Partitioning algorithms-Floor planning concepts –shape functions and floor plan sizing –Floorplanning based on Simulated Annealing		
Unit - III	**Routing and Compaction:**	**9**
Routing – Types of local routing problems – Area routing – channel routing – global routing –algorithms for global routing. Compaction-Layout Compaction –Design rules –problem formulation –algorithms for constraint graph compaction.		
Unit - IV	**Logic Simulation**:	**9**
Simulation –Gate-level modeling and simulation –Switch-level modeling and simulation . Introduction to Combinational Logic Synthesis –Binary Decision Diagrams –ROBDD- ROBDD principles, implementation, construction and manipulation.		
Unit - V	**High level Synthesis** :	**9**
Hardware models –Internal representation –Allocation assignment and scheduling –Simple scheduling algorithm –Assignment problem –High level transformations.		

Lecture:45,Total:45

REFERENCES:

1	Gerez, S.H., “Algorithms for VLSI Design Automation”, John Wiley & Sons, New York, 2002
2	Sherwani, N.A., “Algorithms for VLSI Physical Design Automation”, Kluwar Academic Publishers, Boston, 2002
3	Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts and properties associated with Graph Theory.	Understanding(k2)
CO2	demonstrate the concepts of Physical Design Process such as partitioning, floor planning, Placement and Routing.	Understanding(K2)
CO3	apply the concepts of design optimization algorithms and their application to VLSI physical design automation.	Applying(k3)
CO4	realize the concepts of simulation and synthesis in VLSI Design automation.	Understanding(K2)
CO5	analyze CAD design problems using algorithmic methods for VLSI physical design automation.	Analyzing(K4)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**

CO1	3		2			
CO2	3		3			
CO3	3		3	3	2	
CO4			3	3	3	
CO5	2	3			3	2

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	15	45	40	-	-	-	100
CAT2	10	45	45	-	-	-	100
CAT3	15	45	35	-	-	-	100
ESE	20	40	40	-	-	-	100

*** ±3% may be varied**

20VLE06 MIXED SIGNAL VLSI DESIGN

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI design**	**II**	**PE**	**3**	**0**	**0**	**3**

Preamble	To build the advanced CMOS VLSI Design with practical aspect of mixed signal VLSI blocks such as data converters using HDL	
Unit - I	**Power dissipation in CMOS:**	**9**
Introduction to Active Filters & Switched capacitor filters: Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad		
Unit - II	**Continuous Time Filters**	**9**

Introduction to Gm - C filters - bipolar transconductors - CMOS Transconductors using Triode transistors, active transistors – BiCMOStransconductors – MOSFET C Filters - Tuning Circuitry - Dynamic range performance -Elementary transconductor building block- First and Second order filters		
Unit - III	**Digital To Analog & Analog To Digital Converters:**	**9**
Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's.		
Unit - IV	**Sigma Delta Converters:**	**9**
Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's		
Unit - V	**Analog And Mixed Signal Extensions To HDL:**	**9**
Introduction - Language design objectives - Theory of differential algebraic equations - the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples-analog extensions to Verilog: Introduction - data types –Expressions – Signals- Analog behavior –Hierarchical Structures –Mixed signal Interaction		

Lecture:45,Total:45

REFERENCES:

1	David A Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2008
2	Rudy van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", Kluwer, 2007.
3	Antoniou, "Digital Filters Analysis and Design", Tata McGraw Hill, 2007
4	Phillip Allen and Douglas Holberg "CMOS Analog Circuit Design", Oxford University Press, 2012.
5	BenhardRazavi, "Data Converters", Kluwer Publishers, 2005.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts of active filters and switched capacitor filters	Understanding(K2)
CO2	comprehend the concepts of continuous time filters and its performance	Understanding(K2)
CO3	analyze Digital To Analog & Analog To Digital Converters	Analyzing(K4)
CO4	examine sigma delta converters	Evaluating(K5)
CO5	design Analog and mixed signal circuits using HDL	Creating(K6)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	3	2			
CO2	2	3	2			
CO3	3		3	2		
CO4	3		3	2		
CO5				2	3	

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	40	30	15	-	-	100
CAT2	10	15	20	25	15	15	100
CAT3	10	15	25	25	25	-	100
ESE	10	15	20	25	15	15	100

*** ±3% may be varied**

20VLE07 LOW POWER VLSI DESIGN

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	VLSI Design Techniques	II	PE	3	0	0	3

Preamble	To design the combinational and sequential circuits with minimum power consumption and to anlayse the various power optimization methods and techniques to reduce power consumption.	
Unit - I	**Power dissipation in CMOS:**	**9**
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design		
Unit - II	**Power optimization :**	**9**

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.		
Unit - III	**Design of Low Power CMOS circuits :**	**9**
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques		
Unit - IV	**Power estimation:**	**9**
Power Estimation techniques – logic power estimation – Simulation power analysis –Probabilistic power analysis.		
Unit - V	**Software design for low power :**	**9**
Sources of Software Power dissipation- Power Estimation- Power Optimization- Automated low power code generation- Codesign for low power		

Lecture:45,Total:45

REFERENCES:

1	Kaushik Roy and S.C.Prasad, “Low power CMOS VLSI circuit design”, Wiley, 2000.
2	DimitriosSoudris, ChirstianPignet, Costas Goutis, “Designing CMOS Circuits for Low Power”, Kluwer, 2002.
3	Gary Yeap, “Practical low power digital VLSI design”, Kluwer, 1998.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	enumerate the different sources of power dissipation in CMOS	Remembering(K1)
CO2	analyze various power optimization technique at circuit level.	Analyzing(K4)
CO3	design of low power circuits at architecture level	Creating(K6)
CO4	use of Simulation and probabilistic method of power analysis	Analyzing(K4)
CO5	perform power estimation and optimization at programming level	Evaluating(K5)

Mapping of COs with POs and PSOs						
COs/POs	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**
CO1		3	2			

CO2	2		3			
CO3			3		2	3
CO4		2			3	
CO5		2		3	2	3

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	40	30	15	-	-	100
CAT2	10	15	20	25	15	15	100
CAT3	10	15	25	25	25	-	100
ESE	10	15	20	25	15	15	100

*** ±3% may be varied**

20VLE08 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	II	PE	3	0	0	3

Preamble	To expose the basics and fundamentals of Electromagnetic Interference and Compatibility in Communication System Design and to know the concepts of EMI Coupling Principles, EMI Measurements and Control techniques and the methodologies of EMI based PCB design.	
Unit - I	**EMI Environment :**	**9**
EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD		
Unit - II	**EMI Coupling Principles:**	**9**
Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling		
Unit - III	**EMI/EMC standards and measurements :**	**9**

Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).		
Unit - IV	**EMI control techniques :**	**9**
Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting		
Unit - V	**EMC design of PCBs :**	**9**
PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models		

Lecture:45,Total:45

REFERENCES:

1	Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1988
2	Paul, C.R., “Introduction to Electromagnetic Compatibility”, John Wiley & Sons, New York, 1992
3	Kodali, V.P., "Engineering EMC Principles, Measurements and Technologies", IEEE Press, London, 1996.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	understand the basics of EMI, EMC parameters	Understanding(K2)
CO2	comprehend the principles of EMI coupling mechanisms	Understanding(K2)
CO3	summarize the EMI/EMC standards and measurement techniques	Understanding(K2)
CO4	interpret EMI control techniques	Applying(K3)
CO5	design EMC PCBs	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3					
CO2	3					

CO3	3	2				
CO4	3	2				
CO5	3	3	2			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	40	30	20			100
CAT2	10	40	30	10	10		100
CAT3	10	40	30	20			100
ESE	10	40	30	10	10		100

*** ±3% may be varied**

20VLE09 RECONFIGURABLE ARCHITECTURES FOR VLSI

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	VLSI Design techniques	II	PE	3	0	0	3

Preamble	To comprehend and apply different reconfigurable architecture in FPGA	
Unit - I	**Device architecture:**	**9**
General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices– Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.		
Unit - II	**Reconfigurable computing architectures and systems:**	**9**
Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management		
Unit - III	**Programming reconfigurable systems:**	**9**

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing		
Unit - IV	**Mapping designs to reconfigurable platforms:**	**9**
The Design Flow - Technology Mapping – FPGA Placement – Datapath composition -Retiming, Repipelining, and C-slow Retiming – Configuration Bit stream Generation.		
Unit - V	**Application development with FPGAs:**	**9**
Implementing Applications with FPGAs -Case Studies of FPGA Applications –Signal Processing -Image Processing -Compression – Bioinformatics Application		

Lecture:45,Total:45

REFERENCES:

1	Scott Hauck and Andre Dehon (Eds.), “Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation”, Elsevier / Morgan Kaufmann, 2008.
2	Maya B. Gokhale and Paul S. Graham, “Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays”, Springer, 2005
3	Christophe Bobda, “Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications”, Springer, 2010.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the different computing and models	Understanding(K2)
CO2	discuss the different reconfigurable computing architecture and systems	Analyzing(K4)
CO3	programming reconfigurable systems	Evaluating(K5)
CO4	mapping the design into different platforms	Evaluating(K5)
CO5	analyze and develop reconfigurable applications	Creating(K6)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3			
CO2			3			
CO3					3	

CO4				3		
CO5	3		3	3		3

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	5	25	40	30			100
CAT2		25	30	25	20		100
CAT3		20	30	20	20	10	100
ESE	5	20	30	20	15	10	100

*** ±3% may be varied**

20VLE10 NATURE INSPIRED OPTIMIZATION TECHNIQUES
(Common to VLSI Design and Embedded Systems)

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	III	PE	3	0	0	3

Preamble	To acquaint and familiarize with different types of optimization techniques, solving optimization problems, implementing computational techniques, abstracting mathematical results and proofs etc.	
Unit - I	**Introduction to Algorithms :**	**9**

Newton's Method – Optimization - Search for Optimality - No-Free-Lunch Theorems - Nature-Inspired Metaheuristics - Brief History of Metaheuristics

Analysis of Algorithms : Introduction - Analysis of Optimization Algorithms - Nature-Inspired Algorithms - Parameter Tuning and Parameter Control

Unit - II	**Simulated Annealing & Genetic Algorithms** :	**9**

Simulated Annealing : Annealing and Boltzmann Distribution - Parameters - SA Algorithm - Unconstrained Optimization - Basic Convergence Properties - SA Behavior in Practice - Stochastic Tunneling

Genetic Algorithms : Introduction - Genetic Algorithms - Role of Genetic Operators - Choice of Parameters - GA Variants - Schema Theorem - Convergence Analysis

Unit - III	**Particle Swarm Optimization & Cat Swarm Optimization:**	**9**

Particle Swarm Optimization : Swarm Intelligence - PSO Algorithm - Accelerated PSO – Implementation - Convergence Analysis - Binary PSO - Problems **Cat Swarm Optimization :** Natural Process of the Cat Swarm - Optimization Algorithm – Flowchart - Performance of the CSO Algorithm		
Unit - IV	**TLBO Algorithm, Cuckoo Search & Bat Algorithms**	**9**
TLBO Algorithm: Introduction - Mapping a Classroom into the Teaching-Learning-Based optimization – Flowchart- Problems **Cuckoo Search** : Cuckoo Life Style - Details of COA – flowchart - Cuckoos' Initial Residence Locations - Cuckoos' Egg Laying Approach - Cuckoos Immigration - Capabilities of COA **Bat Algorithms** - Echolocation of Bats - Bat Algorithms – Implementation - Binary Bat Algorithms - Variants of the Bat Algorithm - Convergence Analysis		
Unit - V	**Other Algorithms**	**9**
Ant Algorithms - Bee-Inspired Algorithms - Harmony Search - Hybrid Algorithms		

Lecture:45,Total:45

REFERENCES:

1	Xin-She Yang, "Nature-Inspired Optimization Algorithms" , Elsevier, 2014
2	OmidBozorg-Haddad , "Advanced Optimization by Nature-Inspired Algorithms" Studies in Computational Intelligence Volume 720
3	SrikantaPatnaik, Xin-She Yang ,Kazumi Nakamatsu, "Nature-Inspired Computing and Optimization Theory and Applications" Springer Series, Vol.10

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	infer the basic concepts of optimization techniques	Understanding(K2)
CO2	identify the parameter which is to be optimized for an application	Analyzing(K4)
CO3	analyze and develop mathematical model of different optimization algorithms	Analyzing(K4)
CO4	select suitable optimization algorithm for a real time application	Applying(K3)
CO5	recommend solutions, analyses, and limitations of models	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2		3	2	
CO2	3	2		3	2	

CO3	3	2		3	2	
CO4	3	2		3	2	
CO5	3	2		3	2	

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	10	40	30	20			100
CAT2	10	30	30	30			100
CAT3	10	40	30	20			100
ESE	10	40	30	20			100

*** ±3% may be varied**

20VLE11 SUPERVISED MACHINE LEARNING ALGORITHMS

(Common to VLSI Design & Embedded Systems)

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	III	PE	3	0	0	3

Preamble	To focus on supervised machine learning algorithms to create simple, interpretable models to solve classification and regression problem.	
Unit - I	**Discriminative Algorithms :**	**9**
Cost function –LMS Algorithm – The normal Equations-Probability interpretation-locally weighted linear regression-logistic regression-generalized linear models-Application to prediction		
Unit - II	**Generative Algorithms :**	**9**
Generative Models: Gaussian Discriminant Analysis(GDA)-Naïve Bayes- Laplace smoothing-Marginal classifier: Support Vector Machine (SVM) as optimal Margin classifier-Application to Classification.		
Unit - III	**Neural Networks:**	**9**

ANN Architecture- Parameter Initialization -Forward Propagation- Activation Functions (Sigmoid,tanh,relu)-Training and Optimization with back propagation-Learning Boolean Functions		
Unit - IV	**Convolutional Neural Networks (CNN) :**	**9**
Convolution kernel-Pooling (Max Pooling, fractional Pooling)-Strides-Fully Connected Layers –Loss functions – MiniBatch Training - Optimization – Application to MNIST image classification		
Unit - V	**Fine Tuning :**	**9**
Regularization: Bias-Variance-Bias-variance Trade off- Initialization of parameters (Xavier)-Cross Validation-Data Augmentation-dropouts-Batch Normalization..		

Lecture:45,Total:45

REFERENCES:

1	Christopher M. Bishop, “Pattern Recognition and Machine Learning”, Springer-Verlag New York. reprint 2010
2	Trevor Hastie, “The Elements of Statistical Learning:Data Mining, Inference, and Prediction”, Second Edition, , Springer.
3	UCI Machine Learning repository: http://archive.ics.uci.edu/ml/index.php

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	analyse and apply discriminative algorithms for classification and regression problems	Analyzing(K4)
CO2	validate a generative model based algorithm for classification and regression problems	Analyzing(K4)
CO3	analyse the designed ANN for a real time application using BPN	Analyzing(K4)
CO4	develop a CNN model for image analysis.	Applying(K3)
CO5	analyse various metrics used in fine tuning supervised learning model	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				3	
CO2	1		2		3	
CO3	1		2		3	

CO4	1				3	
CO5	1	3				

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	6	53	24	16			100
CAT2	6	53	24	16			100
CAT3	6	66	28				100
ESE	4	60	20	16			100

*** ±3% may be varied**

20VLE12 SIGNAL AND IMAGE PROCESSING FOR REAL TIME APPLICATIONS

(Common to VLSI Design and Embedded Systems)

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	III	PE	3	0	0	3

Preamble	To develop the image processing tools from scratch, rather than using any image processing library functions.	
Unit - I	**Digital Image Fundamentals**:	**9**

Elements of digital image processing systems- Brightness- Contrast- Hue- saturation- Mach band effect -2D Image sampling- 2D Image transforms: DCT – KLT – Haar. Image Enhancement:Basic intensity transformations – Histogram equalization - Spatial filtering : Smoothing and sharpening Filters – Frequency domain filtering : Smoothing and sharpening filters – Homomorphic filters

Unit - II	**Morphological Image Processing:**	**9**

Erosion – Dilation – Duality – Opening – Closing – Hit or Miss Transformation– Basic Morphological Algorithms : Boundary Extraction- Hole filling – Extraction of connected components – Thinning – Thickening – Grayscale Morphology – Morphological smoothing – Morphological gradient – Tophat and bottom hat transformation

Unit - III	**Image Segmentation:**	**9**

Point, line and edge detection – Basics of intensity thresholding – Region based segmentation: Region growing - Region splitting and merging.Image Compression:Fundamentals: Types of redundancy – Huffmann – Run length coding – Arithmetic coding - Block Transform coding		
Unit - IV	**Pattern recognition :**	**9**
Patterns and Pattern classes – Representation of Pattern classes – Approaches to object recognition :Baye's Parametric classification – Template matching method – Structural Pattern Recognition : statistical and structural approaches		
Unit - V	**Overview of speech processing :**	**9**
Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Short time Homomorphic Filtering of Speech; Linear Prediction (LP) analysis: Basis and development, LPC spectrum.		

Lecture:45,Total:45

REFERENCES:

1	Gonzalez.R.C&Woods.R.E,—Digital Image Processing‖, 4th Edition, Pearson Education, 2009
2	Jayaraman.S, Esakkirajan.S, and Veerakumar.T, —Digital Image Processing‖, Tata McGraw-Hill, New Delhi, First Edition, 2009.
3	Hayes, Monson H. "Statistical Digital Signal processing and Modeling", John Wiley and Sons, Inc., 1996

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	interpret the basic image processing spatial domain characteristics of digital images	Understanding(K2)
CO2	apply Haar, DCT and KL Transforms to transform from spatial domain to other domains	Applying(K3)
CO3	apply morphological operators and segmentation algorithms to extract the edges and regions of interest	Applying(K3)
CO4	employ Huffmann, Arithmetic, Runlength and nblock transform coding techniques and compress the images	Applying(K3)
CO5	Outline the pattern recognition and speech processing approaches	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1			3	3		
CO2			3	2		

CO3	2		3	3		
CO4	2		3	3		
CO5			2	3		

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	40	40				100
CAT2	20	30	50				100
CAT3	20	30	40	10			100
ESE	20	30	40	10			100

*** ±3% may be varied**

20VLE13 RF CIRCUIT DESIGN

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Analog IC Design	IV	PE	3	0	0	3

Preamble	To infer the concepts of CMOS RF circuits and to design RF devices, circuits, and systems at microwave regime.	
Unit - I	**I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES:**	**9**
Introduction to MOSFET Physics, Noise: Thermal, shot, flicker, popcorn noise, Two port Noise theory, Noise Figure, THD, IP2, IP3, Sensitivity, SFDR, Phase noise - Specification distribution over a communication link, Homodyne Receiver, Heterodyne Receiver, Image reject, Low IF Receiver Architectures Direct up conversion Transmitter, Two step up conversion Transmitter		
Unit - II	**IMPEDANCE MATCHING AND AMPLIFIERS:**	**9**
S-parameters with Smith chart, Passive IC components, Impedance matching networks, Common Gate, Common Source Amplifiers, OC Time constants in bandwidth estimation and enhancement, High frequency amplifier design, Power match and Noise match, Single ended and Differential LNAs, Terminated with Resistors and Source Degeneration LNAs.		
Unit - III	**FEEDBACK SYSTEMS AND POWER AMPLIFIERS :**	**9**

Stability of feedback systems: Gain and phase margin, Root-locus techniques, Time and Frequency domain considerations, Compensation, General model – Class A, AB, B, C, D, E and F amplifiers, Power amplifier Linearization Techniques, Efficiency boosting techniques, ACPR metric, Design considerations		
Unit - IV	**MIXERS AND OSCILLATORS:**	**9**
Mixer characteristics, Non-linear based mixers, Quadratic mixers, Multiplier based mixers, Single balanced and double balanced mixers, subsampling mixers, Oscillators describing Functions, Colpitts oscillators Resonators, Tuned Oscillators, Negative resistance oscillators, Phase noise.		
Unit - V	**PLL AND FREQUENCY SYNTHESIZERS:**	**9**
Linearised Model, Noise properties, Phase detectors, Loop filters and Charge pumps, Integer-N frequency synthesizers, Direct Digital Frequency synthesizers		

Lecture:45,Total:45

REFERENCES:

1	T.Lee, “Design of CMOS RF Integrated Circuits”, Cambridge, 2004.
2	B.Razavi, “RF Microelectronics”, Pearson Education, 1997.
3	Jan Crols, MichielSteyaert, “CMOS Wireless Transceiver Design”, Kluwer Academic Publishers,1997.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	differentiate the noises associated with CMOS technology and to comprehend the RF receive operation	Understanding(K2)
CO2	design the input and output impedance matching networks for amplifier design	Applying(K3)
CO3	Illustrate the RF power amplifier design with the context of stability	Applying(K3)
CO4	Interpret the design of RF mixers and oscillators for IC implementation	Understanding(K2)
CO5	comprehend PLL and synthesizer architectures and their performance	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	2				
CO2	3	3	1	1		
CO3	3	2	1	1		

CO4	2	2	1			
CO5	2	2	1			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	20	65	15				100
CAT2	15	60	15	10			100
CAT3	15	60	25				100
ESE	20	60	10	10			100

*** ±3% may be varied**

20VLE14 MEMS DESIGN

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	Nil	IV	PE	3	0	0	3

Preamble	This course equips the students to understand the concepts of Micromechatronics and apply the knowledge of micro fabrication techniques for various applications.	
Unit - I	**Materials for MEMS and Scaling Laws:**	**9**
Overview - Microsystems and microelectronics - Working principle of Microsystems – Si as a substrate material - Mechanical properties - Silicon compounds - Silicon piezoresistors - Gallium arsenide - Quartz-piezoelectric crystals - Polymer -Scaling laws in Miniaturization.		
Unit - II	**Micro Sensors, Micro Actuators:**	**9**
Micro sensors – Types- Micro actuation techniques- Microactuators – Micromotors – Microvalves – Microgrippers – Micro accelerometer – introduction – Types - Actuating Principles, Design rules ,modeling and simulation, Verification and testing – Applications.		
Unit - III	**Mechanics for Microsystem Design:**	**9**

Static bending of thin plates - Mechanical vibration - Thermo mechanics - Thermal stresses - Fracture mechanics - Stress intensity factors, fracture toughness and interfacial fracture mechanics-Thin film Mechanics-Overview of Finite Element Stress Analysis.		
Unit - IV	**Fabrication Process and Micromachining:**	**9**
Photolithography - Ion implantation - Diffusion – Oxidation – CVD - Physical vapor deposition - Deposition by epitaxy - Etching process- Bulk Micro manufacturing - Surface micro machining – LIGA –SLIGA.		
Unit - V	**Micro System Design, Packaging and Applications:**	**9**
Design considerations - Process design - Mechanical design – Mechanical Design using Finite Element Method-Micro system packaging – Die level - Device level - System level – Packaging techniques - Die preparation - Surface bonding - Wire bonding – Sealing - Applications of micro system in Automotive industry, Bio medical, Aerospace and Telecommunications – CAD tools to design a MEMS device.		

Lecture:45,Total:45

REFERENCES:

1	Tai-Ran Hsu, “MEMS and Microsystems Design and Manufacture”, Tata McGraw-Hill, New Delhi, 2008.
2	Mohamed Gad-el-Hak, “The MEMS Hand book”, CRC press, 2009.
3	M.-H. Bao, “Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes”, Elsevier, New York, 2000.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	acquire knowledge about concepts of MEMS materials and Scaling laws	Remembering(K1)
CO2	understand the principles Micro Sensors and Actuators	Understanding(K2)
CO3	gain knowledge about mechanics for microsystem	Understanding(K2)
CO4	know the microfabrication and micromanufacturing techniques	Understanding(K2)
CO5	apply the knowledge to design a microsystem for various applications.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3	3				
CO2	3	3				
CO3	3	3				

CO4	3	3				
CO5	3	3		2		

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	30	70					100
CAT2	20	50	30				100
CAT3	20	50	30				100
ESE	20	50	30				100

*** ±3% may be varied**

20VLE15 VLSI FOR IOT SYSTEMS

Programme & Branch	M.E-VLSI DESIGN	Sem.	Category	L	T	P	Credit
Prerequisites	VLSI Design Techniques	IV	PE	3	0	0	3

Preamble	To infer the components of IOT and integrate it to integrated circuits to design an electronic system	
Unit - I	**INTRODUCTION:**	**9**
Concept of connected world - Need, Legacy systems for connected world-features and limitations, Key features of IoT architecture, Merits and Demerits of IoT technology. Applications driven by IoT technology – examples		
Unit - II	**COMPONENTS OF IOT**:	**9**
Reviewof classic embedded system architecture, Basic building blocks of an IoT system - Artificial Intelligence, Connectivity. Sensors and Computing nodes. Sensors used in IoT systems - Characteristics and requirements. Types of sensors propertiesfor IoT systems, Compute nodes of IoT Connectivity technologies in IoT - Software in IoT systems - features and properties		
Unit - III	**IC TECHNOLOGY FOR IOT**:	**9**
SoC architecture for Iot Devices - Application Processors, Microcontrollers, Smart Analog, Memory architecture for IoT - Non Volatile Memories (NVM). Embedded Non-Volatile Memories, Anti-Fuse One Time Programmable (OTP) memories, Power Management - Low Dropout Regulator, DC-to-DC Converters, Voltage References, Power Management Units (PMUS) in IC's and Systems, Role of Field Programmability in IoT systems.		
Unit - IV	**ELECTRONIC SYSTEM DESIGN FOR IOT**:	**9**

Electronic System Design for IoT Requirements, Computing blocks in IoT systems - MCU's, DSPS and FPGA, System Power Supply Design for IoT systems, Mixed Signal challenges in hardware systems, Form Factor- Guidelines and prevailing standards, Component models & System Design - Feasibility and challenges, System Level Integration, Operating conditions of IoT devices and impact on Electronic System Design, Hardware Security issues, EMI/EMC, SI/P) and Reliability Analysis in IOT systems.		
Unit - V	**APPLICATIONS:**	**9**
Automated Design of Reconfigurable Microarchitectures for Accelerators Under Wide-Voltage Scaling - Approximate Adder Circuits Using Clocked CMOS Adiabatic Logic (CCAL) for IoT Applications -Battery Management Technique to Reduce Standby Energy Consumption in Ultra-Low Power IoT and Sensory Applications		

Lecture:45,Total:45

REFERENCES:

1	Alloto. "Enabling the Internet of Things- From Integrated Circuits to Integrated Systems", Springer Publications, First Edition, 2017.
2	Pieter Harpe, Kofi A. A Makinwa, Andrea Baschirotto, "Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design". Springer International Publishing AG, 2017
3	Rashid Khan, Kajari Ghosh dastidar, AjithVasudevan, "Learning lot with Particle Photon and Electron". Packt Publishing Limited (Verlag), 2016.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	recall the basic concepts of IOT	Understanding(K2)
CO2	infer the components of IOT	Applying(K3)
CO3	understand the IC technology for IOT	Understanding(K2)
CO4	acquire the electronic system design for IOT	Applying(K3)
CO5	infer the applications of IOT	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			
CO2	2		3			
CO3	2		3			

CO4	2		3			
CO5	2		3			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	20	60	20				100
CAT2	20	50	30				100
CAT3	20	50	30				100
ESE	20	50	30				100

*** ±3% may be varied**

20VLE16 QUANTUM INFORMATION AND COMPUTING

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**Nil**	**IV**	**PE**	**3**	**0**	**0**	**3**

Preamble	To infer the concepts of quantum information theory (qubits, quantum gates, and qubit systems) and to discuss quantum algorithms and physical realization of such system.	
Unit - I	**Introduction:**	**9**
Global perspectives - Linear algebra - The postulates of quantum mechanics -Application: superdense coding - EPR and the Bell inequality		
Unit - II	**Quantum circuits:**	**9**
Single qubit operations - Controlled operations – Measurement - Universal quantum gates - Quantum circuit model of computation - Simulation of quantum systems		
Unit - III	**Quantum algorithms:**	**9**
The quantum Fourier transform - Phase estimation – Order finding and factoring - The quantum search algorithm		
Unit - IV	**Quantum Information:**	**9**

Quantum information theory - Quantum error-correction - Fault-tolerant quantum computation - Quantum cryptography		
Unit - V	**Quantum computers (physical realization):**	**9**
Guiding principles - Conditions for quantum computation - Optical photon quantum computer - Optical cavity quantum electrodynamics - Ion traps - Nuclear magnetic resonance - Other implementation schemes		

Lecture:45,Total:45

REFERENCES:

1	Michael A. Nielsen & Isaac L. Chuang, “Quantum Computation and Quantum Information”, Cambridge University Press, 10th Anniversary Edition, 2010.
2	Eleanor G.Rieffel, Wolfgang H.Polak, “Quantum Computing: A Gentle Introduction” , MIT Press, 2011.
3	Scott Aaronson, “Quantum Computing since Democritus”, Cambridge University Press, 2013.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	describe the quantum mechanics using linear algebra	Understanding(K2)
CO2	familiar with qubits and designing of quantum gates	Applying (K3)
CO3	realize the quantum parallelism by using simplest quantum algorithms	Applying (K3))
CO4	understand real-world quantum information processing	Understanding(K2)
CO5	acquire a basic knowledge on physical realization	Understanding(K2)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		2			
CO2	3		3			
CO3	3		3			
CO4	3		2			
CO5	3		2			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	40	40	20	-	-	-	100
CAT2	30	50	20	-	-	-	100
CAT3	30	70	-	-	-	-	100
ESE	30	50	20	-	-	-	100

*** ±3% may be varied**

20VLE17 SYSTEM ON CHIP

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**VLSI Design Techniques**	**IV**	**PE**	**3**	**0**	**0**	**3**

Preamble	To infer the concepts of hardware and software on a chip and to discuss the applications and implementations of system on chip using different communication architectures	
Unit - I	**SOC Introduction**:	**9**
Components of SOC- Design flow – Nature of Hardware & Software, driving factors for hardware- software co design -design space, system specification and modeling – Hardware software trade offs-Co-design approaches- Models of Computation		
Unit - II	**Measurement of Multiple Qubit States:**	**9**
Dirac notation - Projection operators - Hermition operator - EPR Paradox and Bell's Theorem - No-Cloning principle - Simple quantum Gates - Applications of simple Gates – Realizing Unitary transformations - Universally approximating set of Gates		
Unit - III	**Mechanics for Microsystem Design:**	**9**
Static bending of thin plates - Mechanical vibration - Thermo mechanics - Thermal stresses - Fracture mechanics - Stress intensity factors, fracture toughness and interfacial fracture mechanics-Thin film Mechanics-Overview of Finite Element Stress Analysis.		
Unit - IV	**IP Based System /design:**	**9**
Types of IP, IP across design hierarchy-IP life cycle- Creating and using IP-Technical concerns on IP reuse-Integration – IP evaluation on FPGA prototypes		
Unit - V	**SOC Implementation:**	**9**
Study of Processor IP, Memory IP, w rapper design-real time operating system(RTOS),peripheral interface and components ,high		

density FPGAs-EDA tools used for soc design -SOC TESTING:Manufacturingtest of SoC :core layer ,system layer, application layer P1500-wrapper standardization SoC test automation (STAT).

Lecture:45,Total:45

REFERENCES:

1	Patrick Schaumont A Practical Introduction to Hardware/Software Co-design, Patrick Schaumont, 2nd Edition, Springer, 2012
2	Michael J Flynn and Wayne Luk, "Computer system Design: System-on-Chip". Wiley-India, 2012
3	SudeepPasricha and NikilDutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	recall the basic concepts of System on Chip	Understanding(K2)
CO2	infer the applications of System on Chip	Applying(K3)
CO3	acquire the knowledge of the communication architectures used in System on Chip	Understanding(K2)
CO4	understand the IP based System design	Understanding(K2)
CO5	infer the implementation of system on chip	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2		3			
CO2	2		3			
CO3	2		3			
CO4	2		3			
CO5	2		3			

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	50	20				100
CAT2	30	50	20				100
CAT3	30	40	30				100
ESE	30	50	20				100

*** ±3% may be varied**

20VLE18 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

(Common to VLSI Design and Embedded system)

Programme & Branch	**M.E.- VLSI Design**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	NIL	**IV**	**PE**	**3**	**0**	**0**	**3**

Preamble	To get familiar with DSP processor architecture and understand the software tools for implementing the real time applications using Embedded DSP processor	
Unit - I	**Fundamentals of programmable DSPs:**	**9**
Multiplier and Multiplier accumulator (MAC) – Modified Bus Structures and Memory access in Programmable DSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals		
Unit - II	**TMS320C67XX Architecture:**	**9**
Fundamentals of Programmable DSPs - Architecture of TMS320C67XX - Buses- Computational Units- -On-chip peripherals- Timers and Interrupts		
Unit - III	**TMS320C67XX Programming:**	**9**
Pipeline operation - Address Generation Units-Memory organization- Memory architecture -Addressing modes and instruction set-assembly language instructions specific to filter applications-ASM Statement within C -C-Callable Assembly Function		
Unit - IV	**DSP Development System**	**9**
Introduction -DSK Support Tools - DSK Board TMS320C67XX Digital Signal Processor - Code Composer Studio -CCS Installation and Support -Initialization/Communication File - Vector File- Linker File - Compiler - Assembler –Linker- Input and Output with the DSK-Introduction TLC320AD535 (AD535) Onboard Codec for Input and Output - PCM3003 Stereo Codec for Input and Output - Programming Examples Using C Code		
Unit - V	**Applications Using TMS320C67XX:**	**9**

FIR Filter applications-Adaptive filter Applications-Image Processing Applications- Communication Applications-Modulation (all applications using Simulink Blocksets)

Lecture:45, Total:45

REFERENCES:

1	Venkataramani, B. and Bhaskar, M., "Digital Signal Processors: Architecture, Programming and Applications", Tata McGraw–Hill, New Delhi, 2003
2	DSP Applications Using C and the TMS320C6x DSK Rulph Chassaing JOHN WILEY & SONS, INC.2002 ISBN 0-471-20754-3
3	TMS320C67x/C67x+ DSP CPU and Instruction Set Reference Guide-Texas Instrumentation, "User guides: www.ti.com

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	Infer the basic concepts of DSP processor	Understanding(K2)
CO2	Illustrate the basic principles and functions of peripheral units to perform real time operations.	Understanding(K2)
CO3	Apply programming concepts to develop simple and real time applications programs using C67XX processor	Applying(K3)
CO4	Apply programming concepts to develop simple and real time applications using C67XX DSK with CCS	Applying(K3)
CO5	Demonstrate the performance of DSP processors for various domain related applications.	Applying(K3)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	2	2	3	3		
CO2	3	3	3	2		
CO3	3	3	3	2		
CO4	3	3	3	2		
CO5		3	3	2		

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY							
Test / Bloom's Category*	**Remembering (K1) %**	**Understanding (K2) %**	**Applying (K3) %**	**Analyzing (K4) %**	**Evaluating (K5) %**	**Creating (K6) %**	**Total %**
CAT1	30	70					100
CAT2	30	40	30				100
CAT3	30	40	30				100
ESE	30	40	30				100

*** ±3% may be varied**

20VLE19 GENETIC ALGORITHM FOR VLSI DESIGN

Programme & Branch	**M.E-VLSI DESIGN**	**Sem.**	**Category**	**L**	**T**	**P**	**Credit**
Prerequisites	**ASIC Design**	**IV**	**PE**	**3**	**0**	**0**	**3**

Preamble	To perform VLSI design optimization, layout generation and chip testing using genetic algorithm for developing efficient computer aided design tools.	
Unit - I	**Introduction:**	**9**
GA Technology-Steady State Algorithm-Fitness Scaling-Inversion		
Unit - II	**Physical Design of VLSI** :	**9**
GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy - Multiway Partitioning.		
Unit - III	**Standard Cell and Macro Cell Placement :**	**9**
Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of GA with other methods-Standard cell placement-GASP algorithm-Macro Cell Placement-unified algorithm.		
Unit - IV	**Macrocell Routing And FPGA Technology Mapping**:	**9**
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures .		
Unit - V	**Power Estimation**:	**9**
Application of GA to Peak power estimation -Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.		

Lecture:45,Total:45

REFERENCES:

1	Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,2014.
2	Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience, 1977
3	Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.

COURSE OUTCOMES: On completion of the course, the students will be able to		**BT Mapped (Highest Level)**
CO1	comprehend the concepts of genetic algorithm	Understanding(K2)
CO2	realize the concepts of Physical Design Process such as partitioning, floorplanning, placement and routing.	Remembering(K1)
CO3	calculate power estimation in VLSI Layout using Genetic Algorithm	Applying(K3)
CO4	apply genetic algorithm for automatic test pattern generation in VLSI circuits	Applying(K3)
CO5	analyze CAD design problems using Genetic algorithm for VLSI physical design automation	Analyzing(K4)

Mapping of COs with POs and PSOs

COs/POs	PO1	PO2	PO3	PO4	PO5	PO6
CO1	3				2	
CO2	3		3			
CO3				3	2	
CO4			3	3	3	
CO5	2	3			3	2

1 – Slight, 2 – Moderate, 3 – Substantial,

BT- Bloom's Taxonomy

ASSESSMENT PATTERN - THEORY

Test / Bloom's Category*	Remembering (K1) %	Understanding (K2) %	Applying (K3) %	Analyzing (K4) %	Evaluating (K5) %	Creating (K6) %	Total %
CAT1	15	55	30	-	-	-	100

CAT2	15	50	35	-	-	-	100
CAT3	15	45	40	-	-	-	100
ESE	20	45	35	-	-	-	100

*** ±3% may be varied**